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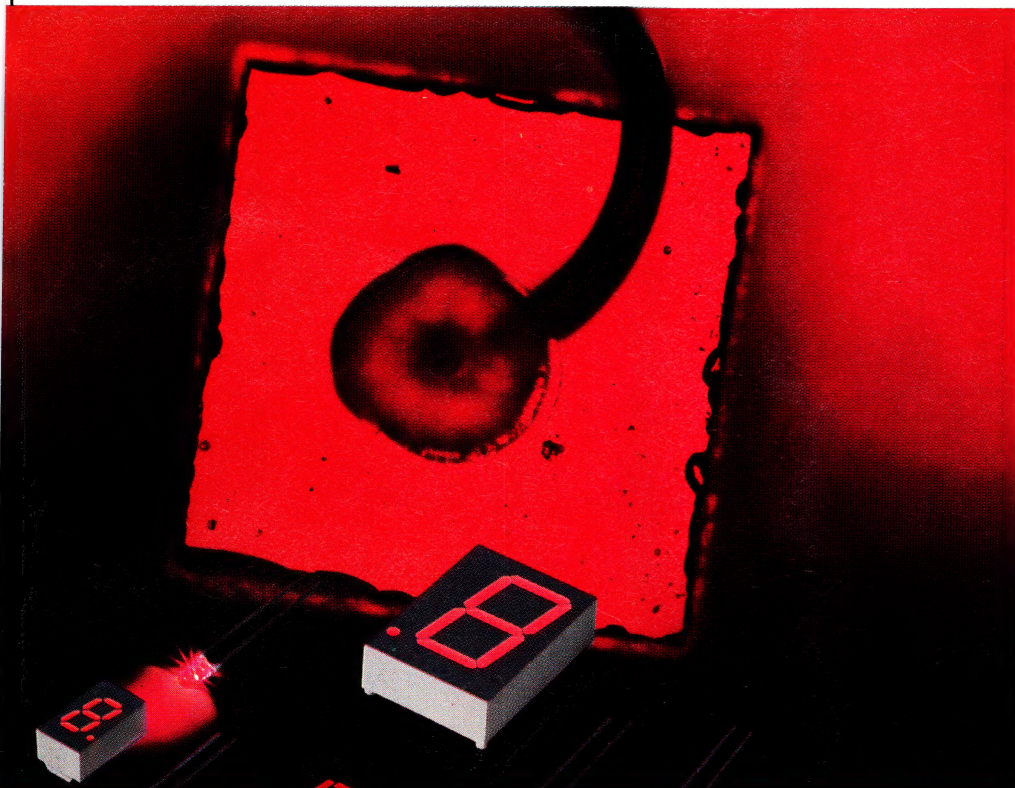
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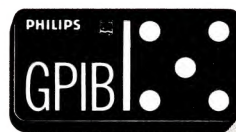
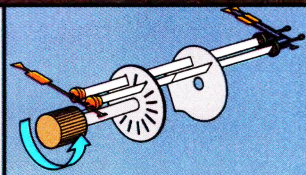
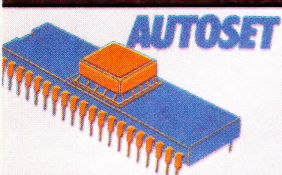
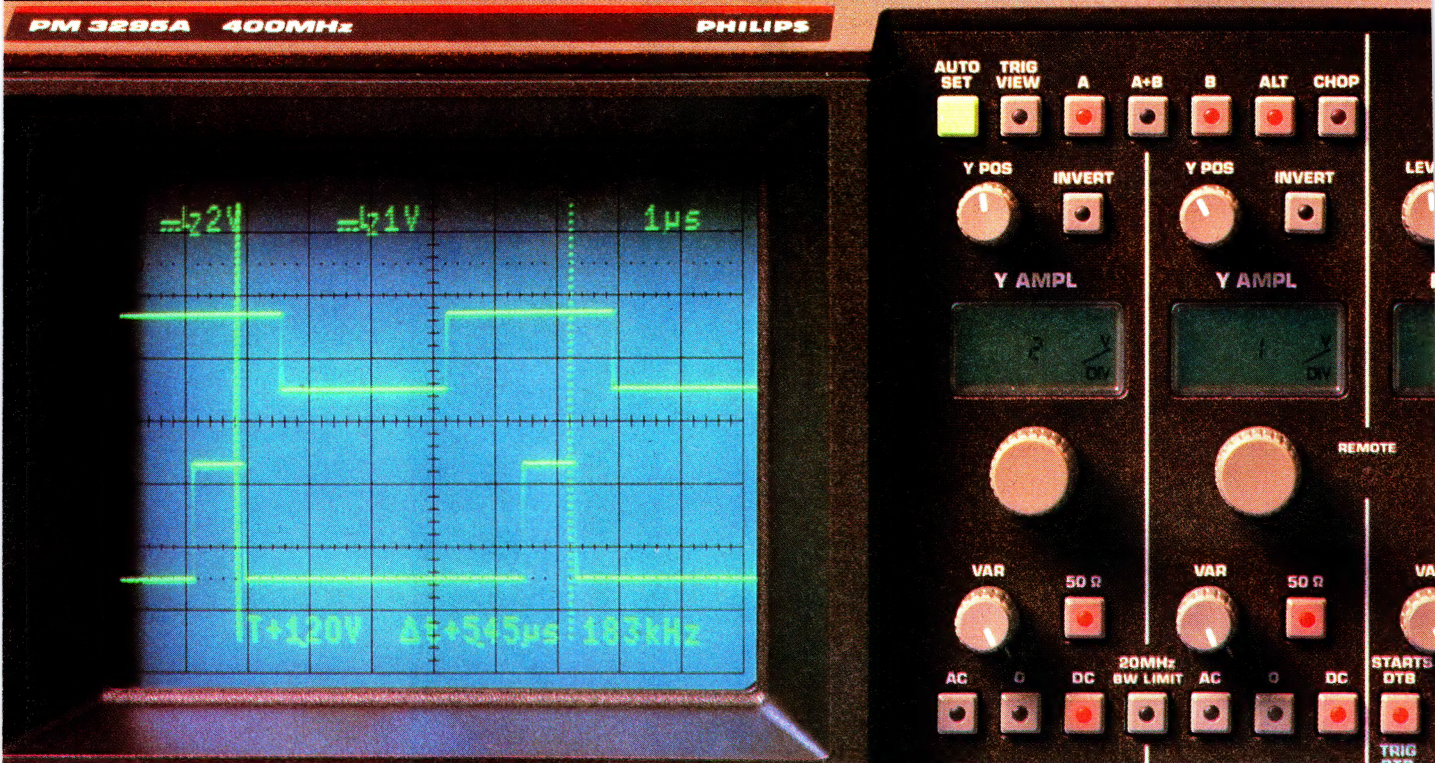
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For some, October means the real beginning of fall. For others, it's the start of the fourth quarter. But for us at *Electronics*, every October since 1974 has meant the season of the annual Technology Outlook.

Our yearly look at what's coming across the whole breadth of the electronic-technology spectrum—an effort that has been much imitated but never equaled—doesn't quite enlist a cast of thousands. But it does require the work of nearly all of the people listed on our masthead. They have spent a lot of time and energy in recent weeks reporting the progress, pulling together the trends, and interpreting the portents in the electronics industry even as they attend to their regular duties in preparing the rest of the issue.

Under the direction of executive technical editor Sam Weber, this 14th annual report, beginning on p. 83, reflects the overarching need that drives technology: more information.

"In every area, from chips to computers to telecommunications, we're seeing faster and more powerful processors, bigger memories, more efficient computer architectures, and more commodious networks," says Sam. And *Electronics* is helping to bring its readers, the people who must satisfy the universal thirst for information, more information that is carefully selected to help them do their jobs.

One way that we carry out that mission is our diligence over the years in keeping step with the ebb and flow of the technological tides. Just consider the changes in the way we divided the tech-



WEBER: Technology is changing faster and faster.

nologies between the Technology Update, as it was then called, of 13 years ago and this year's Technology Outlook.

In 1974, we covered seven specialties: computers, communications, instruments, industrial electronics, consumer electronics, solid state, and components. Now, the count is 12: what was computers in 1974 has split into that category plus software, CAD/CAE, and data communications. Communica-

tions, the former industrial electronics has evolved into factory automation, and we have added chip processing, packaging, and test and measurement. And solid state is now semiconductors and microprocessors. Consumer electronics is the only category untouched.

Another difference is in the choices facing the equipment designer. In 1974, they were more basic than they are now: the engineer had to decide whether to use bipolar or MOS, microprocessors or minicomputers, hard-wired controls or programmable computers. That was pretty much the extent it. But one thing hasn't changed. As we wrote 13 years ago, "For a technology to succeed, the cost must be right, and above all, the timing must be right."

There also has been a quantum change in the pace of innovation over the years. Talking about this year's effort, Sam sums it up this way: "Developments on the technology front move a lot faster now than they did a decade ago. Our editors must not only pick up trends, but they must also be fast on their feet. It is impossible to relax one's guard for a minute."

Laurence Altman

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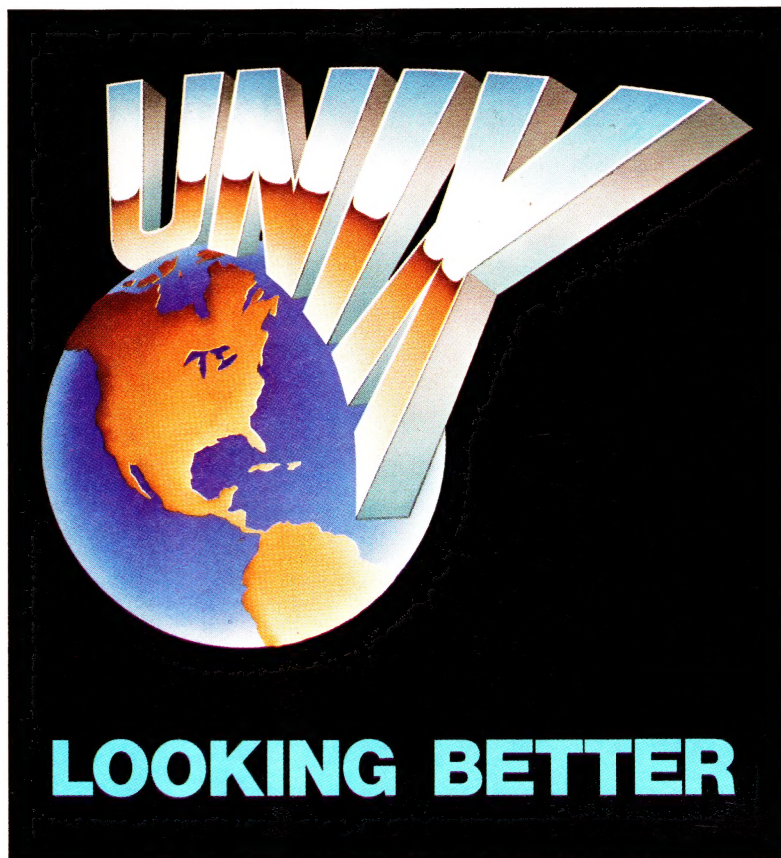
- Western Digital launches a barrage of PS/2 clone chips and boards
- 10-Mbyte 3½-in. floppy-disk drive from Brier Technology runs as fast as a Winchester
- NeuralWare's software package helps engineers to design neural networks
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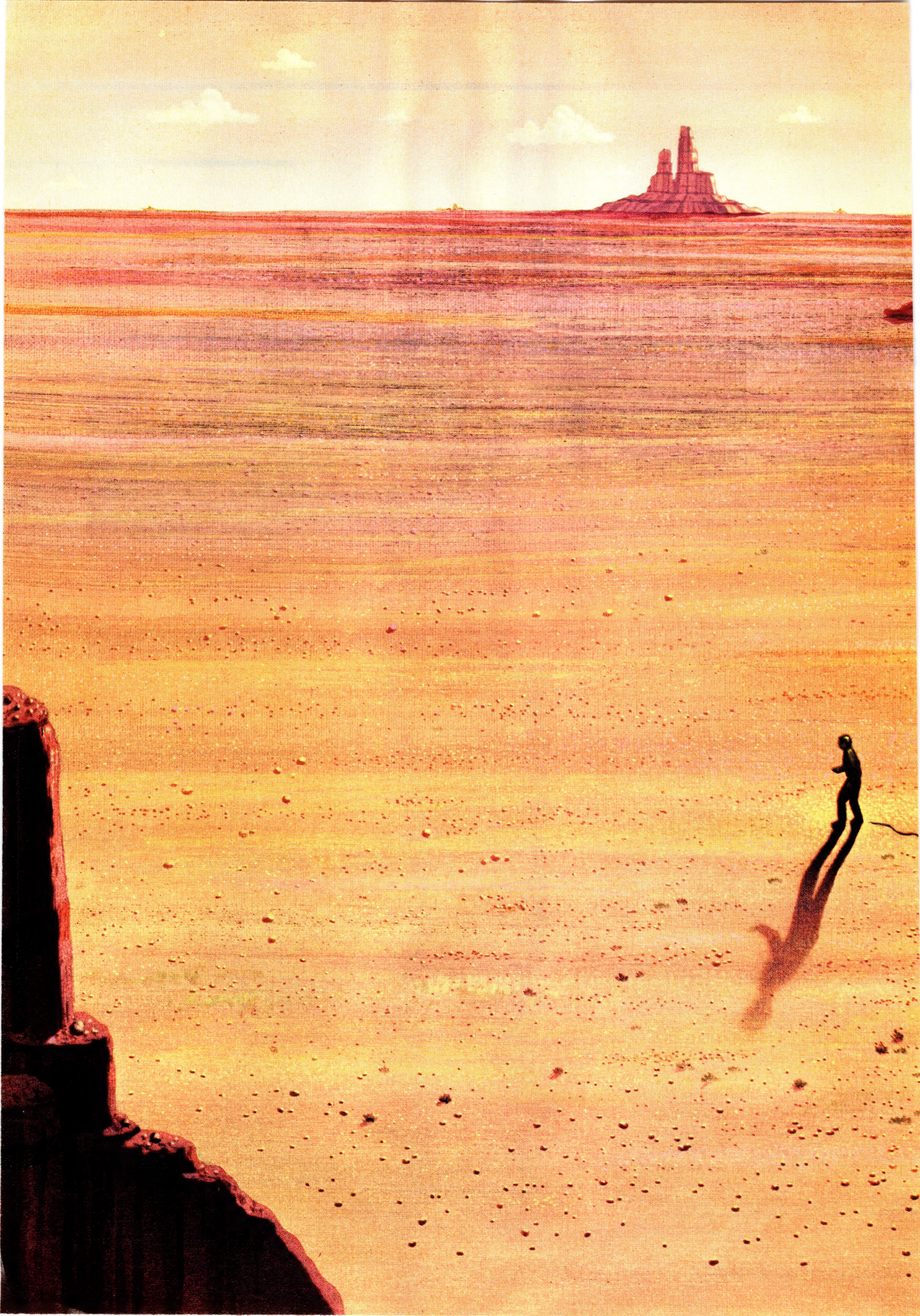
INTERNATIONAL

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- Japan: Casio enters DAT and VCR markets
- Japan: Toshiba is set to sell a 3-d camcorder
- Germany: Bundespost orders a fast fiber-optic link
- Scandinavia: Finns, Swedes get videophone link
- Turkey: The PTT buys Siemens digital switches
- UK: Plessey, Telenet join forces in a datacom venture

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- Two 1.5- μ m CMOS chips do all the decoding and slash power dissipation for Philips's stereo compact-disk player for cars
- A spectrum analyzer from Anritsu handles signals from 10 KHz to 2.2 GHz and offers plug-in memory cards, too
- MORS Components' subminiature switches for PC boards shrug off solder cleaning





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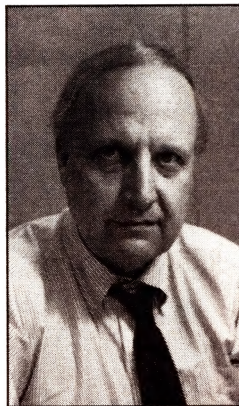
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FYI

OCTOBER 15, 1987

Silicon Valley is really jumping; and we found what we were looking for: company startups and semiconductor development efforts are going full blast



My record still stands: I've been deep inside Lotusland during every major earthquake that's hit that state since the day in 1957 when I ran out onto Bush street after the San Andreas fault rocked San Francisco. Last week's shaker was no sweat for me; I was 400 miles away in Silicon Valley when it blasted President Nixon's birthplace. I was deeply involved in another kind of excitement, though. An editorial team from *Electronics* was spending the week visiting a dozen semiconductor makers to find out what's going on

now in the chip business. The chip guys are creating their own tremors; people feel good about business for a change.

Countering what some publications, such as the *New York Times*, have published recently about the Silicon Valley Blues, the joint was really jumping. We found what we were looking for: startups and product-development efforts were going full blast. Companies that were either located in someone's garage or didn't even exist before the recent downturn are popping up all over the valley. New ideas abound!

How about Actel Corp., less than two years old, whose upcoming CMOS gate-array family will be based on brand-new customer-configurable technology and a proprietary architecture. And how about startup Integrated Device Technology Inc., which will do a nifty \$120 million in its current fiscal year, and expects to do \$200 million in the following year. IDT has even put a lid on growth! "We're limiting our growth to 50% annually, because we can't grow management any faster," declares Larry T. Jordan, vice president. IDT is moving fast; it's now doing all of its designs in submicron technology.

Giant factories are still going up, too. The Japanese—Fujitsu and NEC, for example—seem to be the most ambitious. NEC, which is now running 27,000 wafers a month at its Roseville, Calif., factory, plans a second plant there that will be twice as big. It may be processing 8-in. wafers by 1990.

Speaking of predictions, like many an industry observer, I often poke fun at the annual chip forecasts made by the Semiconductor Industry Association. These gushing predictions have rarely had anything to do with reality. But this year's prediction, made last week in Silicon Valley, was in the same ball park as those numbers coming from other market forecasters. The SIA expects the U.S. to show annual increases in semiconductor shipments of about 20% in 1987 and 1988; that's even below some forecasts.

ROBERT W. HENKEL

SIEMENS

Color: white – Size: SO8 Distinguishing feature: coupler

Experts anticipate that by the year 1990 about 50% of all printed circuit assemblies will be populated with SMDs. The advantages are obvious:

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Circle 174 on reader service card





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PEOPLE

FOR APPLITEK'S HOLSWADE, U.S. SALES ARE JOB NO. 1

WAKEFIELD, MASS.

Negotiating government contracts is a ticklish and often arduous process, one best learned on the job. So local-area-network supplier Applitek Corp., which does 70% to 80% of its business with federal agencies, placed government-contract experience ahead of LANs on its list of criteria for a new president and chief executive officer. In Larry H. Holswade, Applitek has found its man.

"Understanding government regulations, procedures, and legal requirements is quite complex—you can just get lost if you don't understand how it moves," says Holswade, 50, who comes to Applitek after three years at Data General Corp. in Westboro, Mass., as general manager of the Federal Systems Division. Before that, he was vice president of government and military products at Dataproducts Corp., a printer maker in Woodland Hills, Calif.

In all, he has spent 20 years running divisions within large computer and communications companies—and building expertise in negotiating complex, long-term government procurement contracts. In landing government business, he says, the key point is "a period of fact-finding, when the potential customer sees what's available in the market." Applitek's task is to make sure the right people "understand our capabilities and the direction of the company. It's one of the least written-about areas: how to access the people who are running through these kinds of thoughts."

Access apparently has been good for the privately held Applitek during the

past two years. The Wakefield, Mass., company has garnered several multi-year contracts from the National Aeronautics and Space Administration, and the Air Force, Army, and Navy for its universal LAN, called UniLAN. Today, its federal business is done directly or through major systems builders such as GTE, Martin Marietta, and EDS.

UniLAN can run at 10 million bits per second and can change dynamically when network traffic patterns change. It can be installed using baseband, broadband, or fiber-optic cable. "Applitek is uniquely suited to the government market," says Holswade. "With their multiplicity of systems and protocols, government agencies need a universal LAN so they don't have to lose their software and hardware investments."

Holswade's job will be to strengthen Applitek's penetration into this highly sophisticated market against competition from larger firms such as Ungermann-Bass and Bridge Communications. "The definition of communications is still transient," says Holswade. "There are a lot of directions being taken and standards evolving—it's an exciting time to be involved."

Holswade plans to maintain Applitek's large research-and-development effort, so that the company can expand its capability of offering a universal interface. Also, for at least the next 18 months he will concentrate marketing efforts on supporting major system builders working on government contracts. Although he admits that "no one is ever completely buffered" from political shifts that can affect federal contracts, Holswade also points out that "when budgets go down, the procurement of some things goes up; our universal link is in a good position."

Although Applitek is a tiny company, with revenues in the \$8 million range, Holswade is not afraid to think big. "The goal is to be a universal supplier," he says. "There are different paths, though. You can decide you want to be in the commodity business, selling through a sales force, distributors, and resellers. That takes a considerable expense, heavy marketing support, and lots of advertising and documentation. Or you can be a technology leader with more engineering and systems-management capability, working in complex environments that demand rapid technical solutions." Holswade says he plans to take Applitek on the latter road to growth.

—Paul Angiolillo



HOLSWADE: Making sure the right people are interested in Applitek's local network.



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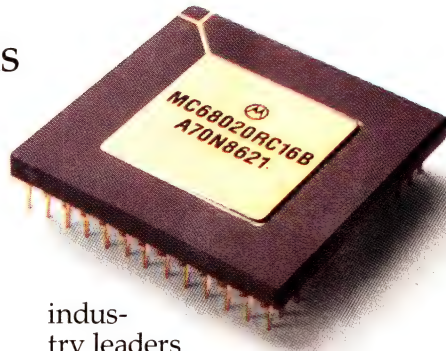
Now Apple has tapped the brainpower of the Motorola MC68020 microprocessor for the Macintosh II, bringing the high performance of a graphics workstation to business desktops everywhere.

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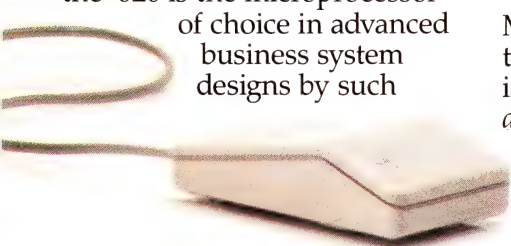
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ELECTRONICS NEWSLETTER

DRAM FIRMS WORRY BOOM MAY SPARK DOUBLE ORDERS AGAIN

Rising prices and orders for 256-Kbit dynamic random-access memories are bringing good times to recession-battered DRAM suppliers—but not without worry that panic buying is behind the recent upsurge. Warning of double and triple orders, John Marck, vice president and general manager of memories at NEC Electronics Inc. in Mountain View, Calif., says NEC's lead times will stretch out to May and June on new orders for 256-Kbit chips. In an effort to keep its lead times short, Texas Instruments Inc. is not taking on any new customers. "We are trying not to take orders past the first quarter," says Ramesh L. Gadwani, manager for TI's U. S. MOS Memory Division in Houston. That's kept TI's prices "stable for the last three months," he adds. But prices in general have not been stable. DRAM prices rose 10 cents a week in September, says one analyst, and prices for 256-Kbit parts could reach \$3, up from less than \$2 a year ago. The trend is likely to continue. NEC's Marck warns that the DRAM shortfall could reach 15% by January. □

NATIONAL INTEGRATES FAIRCHILD'S OPERATIONS WITH ITS OWN...

For National Semiconductor Corp., the hard part of its deal to buy Fairchild Semiconductor Corp. has only just begun. After signing the final agreements, delayed for a week to work out the details, National will face the monumental task of gluing the two companies together—a job it has given itself just a half year to complete. James M. Smaha, executive vice president of National's Semiconductor Group, says speed in completing the merger is essential to keeping Fairchild's top technologists and executives from defecting. Some key personnel have already quit, however, and worry is building as Fairchild's 9,000 employees anticipate layoffs. □

... AND FAIRCHILD'S CUSTOMERS RETURN TO THE FOLD

While executives at National Semiconductor Corp. worry about how to bring Fairchild into its fold, Fairchild product managers say customers are already responding positively to the merger. Clients who were unsure of Fairchild's future after Fujitsu Ltd.'s aborted attempt to purchase the company last winter are now beginning to commit to new products and technologies, especially Aspect, Fairchild's newest LSI emitter-coupled-logic bipolar process. Chip-buying computer houses were holding off committing to Aspect-based products while the fate of the company remained in limbo. Now "we are really encouraged," says Tom Miller, director of strategic marketing for Fairchild's custom and microprocessor unit. "Up until the first of September, we could not get anyone to commit [to Aspect]." But during that month, Fairchild won two customer commitments, and Miller says he is close to signing eight more in the next 60 days. □

NEW CONSORTIUM WILL FUND PRODUCTION-TECHNOLOGY RESEARCH

A new consortium of U. S. manufacturers seeking to improve their competitiveness in world markets is taking aim at control technology. The National Center for Manufacturing Sciences of Ann Arbor, Mich., was established to solve generic manufacturing problems that are too costly for its 225 member companies to finance individually. These include electronic controllers, sensor and control techniques, and test-and-evaluation methods. Edward Miller, the consortium's executive director, says the group will spend between \$60 million and \$100 million over the next three to five years on a project aimed at improving control technology, which is crucial to automated manufacturing. Miller says electronic controllers have not "evolved with other state-of-the-art technology." □

ELECTRONICS NEWSLETTER

ETA SYSTEMS WILL UNVEIL LOW-END SUPERCOMPUTERS THIS WEEK...

Look for ETA Systems Inc. to make a major thrust in the supercomputer arena this week by announcing a new line of lower-performance, air-cooled machines based on the same technology as its eight-processor, liquid-nitrogen-cooled ETA¹⁰. Pricing on the systems, though not yet disclosed, could start at \$2 million or less. The idea is to take advantage of the speed of the 20,000-gate CMOS array chips that the St. Paul, Minn., company buys from Honeywell Inc. for the ETA¹⁰. Chips that don't meet speed specifications for the ETA¹⁰ will be used in the less powerful and less costly air-cooled systems. These machines will use the same single-board processors as the ETA¹⁰, and will come with various clock speeds and in models using from one to eight processors. □

...AND PUT PRESSURE ON ALLIANT, CONVEX, AND FLOATING POINT

The new line of air-cooled machines from ETA Systems Inc. could put extra pressure on minisupercomputer makers such as Alliant Computer Systems, Convex Computer, and Floating Point Systems. These companies produce machines that start at around \$1 million, but offer lower performance than the new series of low-end ETA supercomputers. ETA aims to take advantage of volume manufacturing efficiencies in building identical processor boards for the entire line at its highly automated St. Paul, Minn., plant. The new entries will also compete with Cray Research Inc.'s \$2.5 million X-MP/14se, [*Electronics*, Feb. 19, 1987, p. 30], which can perform about 250 million floating-point operations per second. □

NEC FINDS A WAY TO TAME X-RAY LITHOGRAPHY...

NEC Corp. has developed a system for performing X-ray lithography with line widths of about 0.2 μm , using the 10 Å unit radiation produced by synchrotron orbital radiation. The development brings Japan closer to West Germany, which now leads in X-ray lithography [*Electronics*, Feb. 5, 1987, p. 78]. Kazuo Ayaki, vice president of NEC's Research and Development Group, says the system will become practical when small synchrotrons now being developed are completed in about three years. It features a 25-mm by 25-mm beryllium window that extracts X-rays with minimal attenuation, permitting wafers to be processed in the atmosphere. That eliminates the need for load locks and permits traditional methods of lubrication in the vertical aligner. Throughput should be 40 8-in. wafers/hr, NEC says. A prototype is in use at Japan's National Laboratory for High Energy Physics at Tsukuba. □

...AS PERKIN-ELMER TARGETS 0.5-MICRON FEATURES OPTICALLY

Perkin-Elmer Corp. will unveil next spring an optical lithography step-and-scan system that will be able to put down 0.4- μm minimum feature sizes on silicon wafers, says Michael Gumpert, an analyst with Drexel Burnham Lambert Inc. in New York. The company will not disclose its plans, however, saying only that it is working on a lithography product that "we think will knock some people's socks off." Gumpert bases his assessment on previously published technical papers, which he says indicate that a system capable of printing a minimum field of 1 sq. in. and at least 0.5- μm resolution is in the offing. Such a system, he says, would increase throughput by as much as six to eight times over current optical lithography steppers. Gumpert says Perkin-Elmer has been testing prototypes at IBM Corp. facilities for two years, but hasn't yet built a production machine. He says the company must "have at least six machines in beta sites by the end of March" if it is to cash in on the wave of orders for chip-making equipment anticipated for 1988. □

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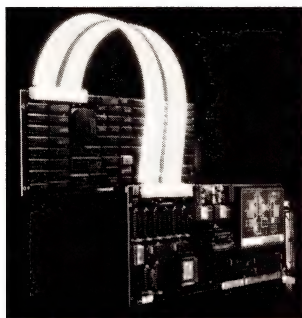
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DT2841-F-16SE	16SE	12	1,2,4,8	150	2	130/chan	16	2	✓	\$2095
DT2841-F8DI	8DI	12	1,2,4,8	150	2	130/chan	16	2	✓	\$2095
DT2841-G-16SE	16SE	12	1,2,4,8	250	2	130/chan	16	2	✓	\$2695
DT2841-G-8DI	8DI	12	1,2,4,8	250	2	130/chan	16	2	✓	\$2695
DT2841-L	4DI	12	1	750	2	130/chan	16	2	✓	\$2995
DT2847	4DI	16	1	100	2	130/chan	16	2	✓	\$2495
DT2848	4SE(2)	12	1	100	2	130/chan	16	2	✓	\$2095

Notes: (1) Throughput shown is per D/A channel. Aggregate throughput is 260kHz. (2) Simultaneous Sample and Hold A/D

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PRODUCTS NEWSLETTER

WESTERN DIGITAL LAUNCHES BARRAGE OF PS/2 CLONE CHIPS AND BOARDS

Computer makers out after a piece of the six-month-old Personal System/2 market opened up by IBM Corp. can count on Western Digital Corp. for considerable help in cutting costs through drastically reduced components counts. Over the next five months, the Irvine, Calif., company will bring to market a family of 19 parts—including a single-chip implementation of the core logic for the PS/2 Models 25 and 30 and a four-chip set for Models 50 and 60. The FE2011 core-logic chip for Models 25 and 30 will be sampled starting in December and priced at \$33 in 100-unit quantities; the FE5400 four-chip set will follow in January, priced at \$99, also in lots of 100. The WD PS/2 family also includes the PVGA1 video graphics controller (available now, \$60); the WD57C65 single-chip floppy-disk interface (available now, \$6); and the WD16C552 single-chip dual-channel asynchronous communications unit (available in February, \$12). Like Chips & Technologies (p. 75), Western also is offering adapter boards compatible with the IBM PS/2 Micro Channel bus found on the PS/2 Models 50, 60, and 80. □

10-MBYTE 3½-in. FLOPPY DRIVE RUNS AS FAST AS A WINCHESTER

A new company called Brier Technology Inc., San Jose, Calif., says it has developed a 3½-in. floppy-disk drive with the capacity and performance of Winchester drives. Previously, only the 5¼-in. floppy-disk drives from Iomega Corp., Roy, Utah, have attained the performance of a Winchester. The Brier product stores 10 Mbytes of data on a conventional disk and accesses in an average of 35 ms—comparable to the speed of 3½-in. Winchesters. Brier plans to show the drive at the 1987 Fall Comdex show to be held in Las Vegas Nov. 2-6. It contains a Small Computer Systems Interface within the 3½-in. form factor, for easy integration into existing systems. Brier expects to ship evaluation units in the second quarter of 1988; when production starts, OEM quantities will go for \$400 to \$500 each. □

SOFTWARE HELPS ENGINEER TO DESIGN A NEURAL NETWORK

An extensively documented software package called NeuralWorks Professional is designed to introduce engineers to neural computing and the design of neural networks for such applications as signal processing, filtering, image and pattern recognition, and fuzzy-logic expert systems. A graphical interface running on an IBM PC XT or AT lets the user develop a concept, then create, edit, train, test, and debug a network using one of eight major neural-network paradigms. The package is said to be simple enough to be used by someone with no experience in neural computing, yet sophisticated enough to solve complex problems. It sells for \$495 and is available now from NeuralWare Inc., Sewickley, Pa. □

FAST 12-BIT TRACK-AND-HOLD AMPLIFIER RUNS ON 5-V SUPPLY

Speedy CMOS 12-bit analog-to-digital and digital-to-analog converters now have a companion fast track-and-hold amplifier that runs from the same ± 5 -V power supplies. Crystal Semiconductor Corp. of Austin, Texas, has a 12-bit self-calibrating track-and-hold, the CS3112, with fast acquisition times—1 μ s to a 0.01% error level—and a typical aperture jitter of 100 ps. The CMOS part is aimed at an emerging analog signal-processing market, where the new CMOS converters are used but matching 5-V track-and-hold circuits cannot be found. Existing parts typically need 15-V supplies. Crystal's 1- μ s chip is priced at \$12.10 each in 100-piece lots, and a device rated for 2- μ s operation at \$8.90 each. The chip has a droop rate of only 0.001 μ V/ μ s, which Crystal says beats the competition by a wide margin. □

PRODUCTS NEWSLETTER

EPLD CHIP BUILDS CUSTOM PERIPHERAL FUNCTIONS QUICKLY

Altera Corp. is introducing a new kind of product it calls a user-configurable microprocessor peripheral device. The Santa Clara, Calif., company's EPB1400 is built around a core of erasable programmable logic and can be used in read/write counters and timers, frequency dividers, configurable input/output ports, and data-communications transceivers. The company plans more such function-specific, programmable-logic chips, which it expects to compete in the application-specific integrated-circuit market as a fast, high-density solution without the high engineering costs, long development cycles, and inventory burdens associated with ASICs. The EPB1400's bus interface, configurable through seven control macrocells, allows it to work with all popular 8-, 16-, and 32-bit microprocessors operating at up to 25 MHz. It sells for \$24.50 in lots of 100 and is available now. ☐

HIGH-END GRAPHICS CARD LETS PCs CHALLENGE WORK STATIONS IN CAD

A high-end graphics card built with a VLSI implementation of Metheus Corp.'s Omega graphics engine will juice up IBM Corp. XT and AT personal computers for computer-aided-design work. It will give them graphics performance comparable to work stations costing much more, which means that PCs can challenge work stations for the engineering market. Selling for \$1,395 and due for shipment this month, the Ultra Graphics Accelerator card has a resolution of 1,024 by 768 pixels with a depth of 4 bits per pixel. It can be used with 60-Hz noninterlaced monitors and draws random vectors at 10 million pixels/s. A number of popular CAD programs operate with the UGA, which offers a better combination of resolution, performance, and price than anything else on the market, says Metheus, of Hillsboro, Ore. ☐

CORTEX'S CASE TOOL USES PICTURES TO GENERATE VAX PROGRAMS

A technique called picture programming can automate most software development for Digital Equipment Corp. VAXes running under VMS. Corvion, from Cortex Corp. of Waltham, Mass., is a computer-aided software-engineering tool that translates diagrams drawn on an IBM Corp. Personal Computer AT into business applications, helping programmers with design, implementation, error-checking, maintenance, and documentation. Using a mouse, pop-up menus, and icons, a developer creates diagrams of multiuser information-processing applications. The software then generates at least 95% of the production-ready code for a program. Corvion is available now for from \$50,000 to \$175,000, depending on the VAX model. ☐

NEC ISDN CHIPS WILL LINK PBX TO USER STATIONS

NEC Corp. in November will begin sampling three CMOS chips that are central to its product line for the integrated services digital network. The ISDN chips will implement the link between a private-branch exchange and an individual workplace, where there will typically be both a digital telephone and a terminal, such as a personal computer. Conforming to CCITT recommendations for ISDN, the chips provide protocol control as well as the two-wire 2B+D interface for the PBX-to-workplace link. The μ PD98001 intelligent interface controller does ping-pong time-division two-way transmission over a two-wire line. The μ PD72107 LAPB controller implements the link-access-procedure-balanced-mode protocol used for the digital-terminal channel. The μ PD72305 LAPD controller handles the protocol for the D (signaling) channel that controls the two B (data) channels. Sample price of the μ PD98001 is \$206; for the μ PD72107 and μ PD72305 it is \$275. ☐

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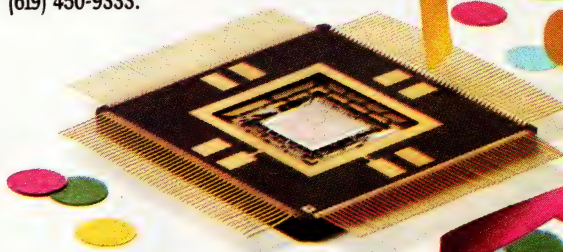
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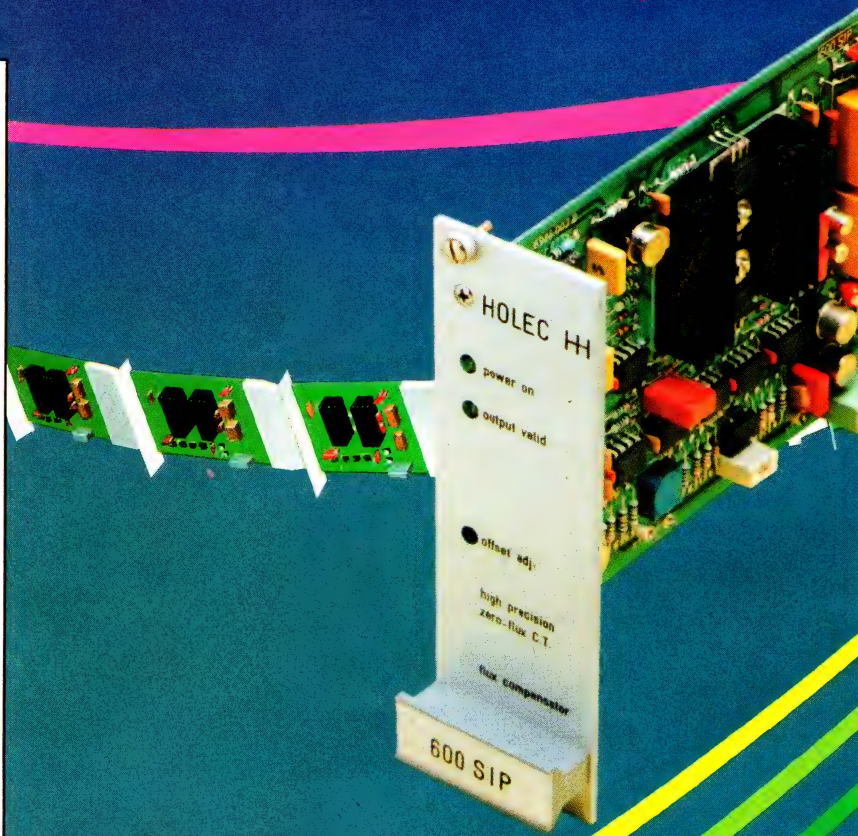
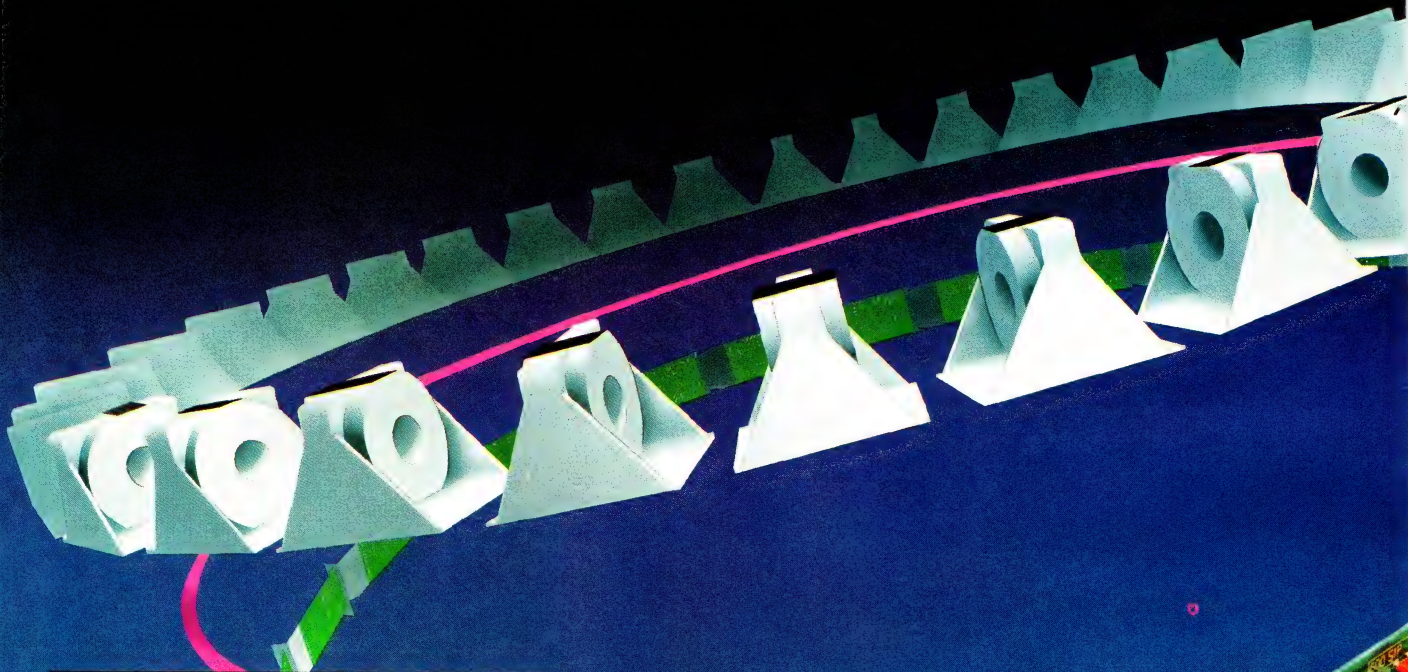
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Problem. A major order for high performance, high precision DCCTs (Direct Current – Current Transformer) called for 100% functional checking of each PCB-based unit. However, the test and measurement set-up should not become redundant once the order had been completed.

Analysis. Essentially, the DCCT is a 600A to 65kA pulsatory current meter with a accuracy of ± 5 ppm. The order (575 units) was for current control of the LEP (Large Electron Positron) at the European Laboratory of Particle Physics, CERN, in Geneva.

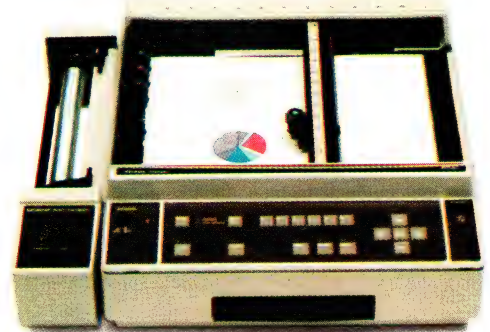


Our customer, Holec – one of the world's leading manufacturers of computerized control equipment for high energy applications, developed a CAT (Computer Aided Testing) system in which a hierarchal instrument controller communicates with a lower-level measurement sub-system via a GPIB-interface. Measurement protocols stored in the controller provide a library of selectable measurement cycles.

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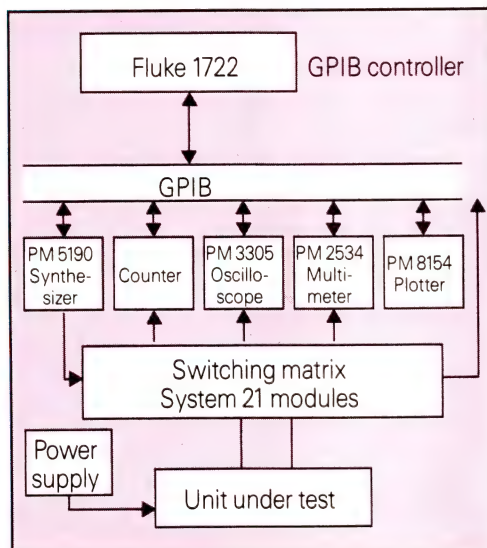
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Electronics

THE SUN COMES OUT FOR DATA GENERAL

NTT PICKS MINI MAKER AS PARTNER TO DEVELOP INTEGRATED NETWORKS

WESTBORO, MASS.

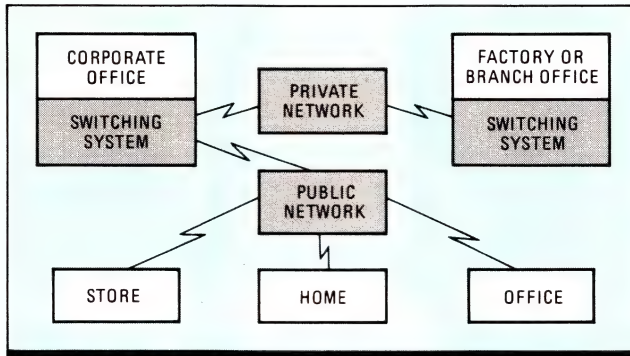
There's good news at Data General Corp. for the first time in many a month. Japanese telecommunications giant Nippon Telegraph & Telephone Corp.'s selection of Data General as its development partner for integrated private data networks is a shot in the arm for the Westboro, Mass., computer manufacturer, which in 1987 will experience the first unprofitable year in its 19-year history [*Electronics*, Sept. 3, 1987, p. 42].

The joint development agreement that NTT and Data General announced last week could be the first of similar affiliations between DG and U.S. and European companies in data networks. What's more, the pact is the first significant endorsement of DG's strategy to catapult into the corporate data-network business through an initiative directed by its 16-month-old Communications Systems Group.

RICH MARKET. The value of the NTT contract wasn't disclosed, but the agreement will open a new market that could be worth several hundred million dollars to the U.S. company. It calls for DG to develop integrated high-speed digital communications systems for NTT. The size and reach of NTT, which controls some 85% of Japanese communications, stamps the DG data-network organization that's evolving under senior vice president Colin Crook as a significant force.

What's more, Crook says, the agreement will help pay for DG's own development of private data-network technology. It calls for DG to deliver by spring of 1989 an integrated communications-processor system and computer system, along with hardware and software interfaces and "all the first-level communications support" required for high-speed digital communications systems, says Crook. Such systems will consist of hybrid exchange units that integrate data, voice, and computers into intelligent private networks.

A system will do more than private switching, points out Yasuharu Kosuge,



COMING FROM DG. Data General will develop hybrid exchange systems that integrate intracompany data communications.

senior engineer and supervisor in NTT's Integrated Communications Systems Sector. If customers select an appropriate processor model, the system will handle switching in a priority mode but will also allow them to run applications software. The computers control both circuit and packet switching over what the Japanese call a superdigital leased line, equivalent to a T1 line from AT&T Co.

Kosuge says that DG will develop interfaces to the line and to Japanese terminals, along with communications software. Kosuge hopes NTT can sell several hundred systems during the first year after development is completed. He says DG was selected for the development because "its hardware is well regarded in Japan, its maintenance and aftercare are excellent, and its communications expertise is superb."

Crook stresses that it was important for DG "to establish our bona fides [in data networks] with a company the magnitude of NTT. It's a good test of how smart we are in this business." In agreement is securities analyst John Adams, chairman of Adams, Harkness & Hill Inc. in Boston. "It's a formidable proposition to enter a relationship of this kind that includes a language barrier, and an unusual way to present your bona fides," says Adams. "But Data General needed somebody substantial to establish its credentials, and NTT is a hell of a choice."

Another analyst notes that the agreement underscores DG's technological

know-how. "It bodes well for Data General that NTT passed up Japanese and other U.S. companies to go with them," says Stephen Zamierowski, who follows the communications industry for International Data Corp. of Framingham, Mass. "It shows that they passed the acid technology test, and it is a vote of confidence that they will be around for a while."

A third analyst is a little more cautious, however. Susie Peterson, who tracks the computer industry for The First Boston Corp. in New York, says the agreement is important for DG in the short term "because it will give them a lot of political good will. But a lot can happen to DG between now and the time they're supposed to deliver. If they're still a stand-alone company, this could be an important product line for them."

DG's Crook points out that NTT has about 5,000 networks installed in Japan among clients that are a veritable who's who of Japanese banks and manufacturing companies. The agreement will open an upgrade-and-replacement market to DG, which has sold minicomputers to NTT through its subsidiary, Nippon Data General, for 15 years.

GETTING TOGETHER. That relationship fostered initial meetings between Crook and other representatives of his group and NTT, during which DG learned that the Japanese giant had established a new group to concentrate on private corporate data networks, just as DG had done. "Over time," Crook relates, "NTT's senior management became impressed with our understanding of the merger of computers and communications. We knew how to position ourselves and our products, and we learned how to do business in Japan."

Crook indicates that other joint efforts will follow, though he declines to offer details. For his part, analyst Adams suggests that Northern Telecom Inc., the Nashville, Tenn., telecommunications leader, might be another logical partner.

—Lawrence Curran

THIS JUST MAY SPEED THE USE OF ROBOTS

DETROIT

Wider use of time-saving robot simulation and off-line programming may be on the horizon after a groundbreaking meeting in Detroit on Oct. 1. The result could be new standards to help overcome one of the fledgling industry's major stumbling blocks: inaccurate modeling of robot arms. And, because simulation cuts the time needed to put together a work cell, that could mean quicker proliferation of robots.

The landmark meeting took place because Deneb Robotics Inc. was frustrated. The tiny Troy, Mich., vendor of robot-simulation systems, tired of trying without success to get information that it needs from robot makers, took the bull by the horns and invited them to discuss the problem.

Such information is vital to Deneb and other firms, whose systems merge robot simulation with the ability to write programs that can be downloaded directly to a robot. They can potentially cut by 70% the time needed to develop a manufacturing work cell [*Electronics*, April 28, 1986, p. 16]. A number of companies, including Computervision, Deneb, GE Calma, Intergraph, McDonnell Douglas, Robcad, and Silma, provide robot-simulation systems.

NO DATA. But a lot of manufacturers don't trust the systems, because sometimes they're not totally accurate. Deneb, for one, concedes that its own \$120,000 Igrip system can be inaccurate. And part of the problem is that robot vendors won't disclose needed data, says Nathan Yoffa, Deneb's director of technical services.

Hence the meeting. General Motors Corp. and Chrysler Corp., which support Deneb's position, sent high-ranking manufacturing executives to the meeting. James Peyton, manager of standards development, represented the Robotics Industries Association, Ann Arbor, Mich. In all, the meeting drew some 90 attendees, including representatives from about 18 robot companies.

Despite contentions to the contrary by some simulation vendors, Deneb executives say that all robot-simulation systems suffer from the same kinds of inaccuracies. Automakers agree with them. At Chrysler, for example, simulation systems from several vendors are used in developing work cells, but not for developing programs that can be downloaded directly to a robot, says William D. Malecki, Chrysler's manager of robotics and automation systems.

The Detroit meeting included a wide-ranging, two-hour open discussion,

which sometimes became heated. Some, such as Bert Thorvaldsson, an executive with Sweden's ASEA Robotics Inc., laid the problem back at the simulation vendors' door. "I have yet to receive a decent requirement sheet from a simulation vendor about [exactly] what it is they want," Thorvaldsson said. Others said that some simulation vendors ask for detailed information that is unavailable, and could be provided only at great cost. Still others, such as Guy Potok, a GMFanuc Robotics Corp. official, said that simulation houses are welcome

to certain basic information. But some detailed characteristics of GMF's robot-control system and Karel robot-programming language give the company a proprietary edge and will never be released, Potok said.

Many agreed that a standard from the RIA could help. And Peyton notes that support by robot users such as GM and Chrysler is likely to carry some weight. "This was definitely a landmark meeting in that it provided the first impetus for standardization in robot simulation," Peyton says.—*Wesley R. Iversen*

MICROPROCESSORS

AT&T GETS GOING WITH NEW 32-BIT CHIP STRATEGY

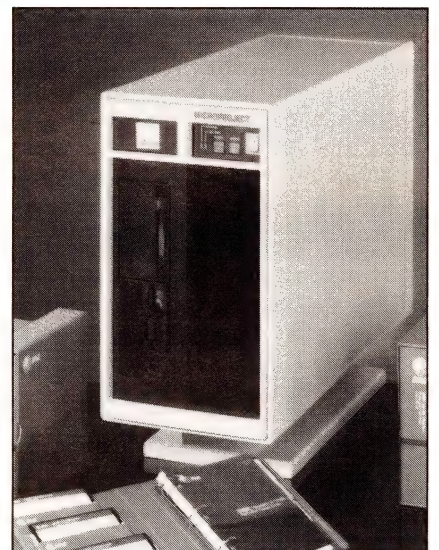
BOSTON

Stymied in its attempts to become a major player in the 32-bit chip business, AT&T Co. is trying a new tack with its WE 32000 microprocessor family. The communications giant is writing off two years of trying to sell directly to chip or board-computer customers, and is going to team instead with small systems-integration firms that will then carry the marketing ball.

"We recognize that [chips and] single-board computers are not a direct marketplace," says John Feaver, technical staff member at AT&T Components and Electronic Systems, Holmdel, N.J. "We need systems integrators who can see what customers need and are much more responsive [to them]."

That's no surprise to analyst Richard A. Shaffer, editor and publisher of the *Technologic Computer Letter*. The way AT&T has been left in the dust by Intel and Motorola in the 32-bit market, it has little choice but to take the systems-integrator road, he says. "AT&T needs visibility, and this is one way to get it."

The first results of the new strategy surfaced last week at Buscon, the computer-board-oriented meeting in Boston, where Microproject International Inc. of Los Angeles and Mizar Inc. of Minneapolis showed new hardware incorporating AT&T products. The technology is impressive. For example, Microproject's Unicorn B/200 computer family has a VMEbus-based processor board that uses for the first time anywhere AT&T's 30-MHz WE 3220X chip set. And Mizar's Unistar-32 VME/Unix multitasking development system will soon have a version with the newest chips. Both already sell versions with the earlier WE 32100 devices.



DEBUT. The Unicorn B/200 is the first computer to use AT&T's 30-MHz 32-bit chip set.

Another first for both computers is that they offer the new V/VME 3.1 version of the widely employed Unix multiuser operating system. Unix users have been anticipating the system's arrival for such features as shared executable libraries, remote file sharing, and media-independent networking.

The Unicorn, aimed at fast throughput and multiuser performance, already has gained about 50 sales. Besides the 30-MHz 32200 processor, which itself is capable of 8 million instructions per second for single users, the design employs a separate Motorola 68020 32-bit processor as a disk controller. The purpose is to reduce bus traffic and speed data transfer between peripherals and main memory. The company offers a range of

configurations, from the 18-MHz eight-user unit at about \$20,000, available now, up to a \$45,000 30-MHz, 50-user version, coming in early 1988.

Microproject's partnership with AT&T—which, like Mizar's, began early this year with little publicity—is an unqualified plus, says Zion Bar-el, execu-

tive vice president for sales. "Our close ties to AT&T give Unicorn B/200 customers prompt access to latest versions of Unix," among other benefits, he says.

Can such relationships turn around AT&T's 32-bit fortunes? Consultant William I. Strauss of Forward Concepts Inc., Tempe, Ariz., gives the company

an outside chance. "By any standard, the 32000 is a good set that has not been marketed well. This [new strategy] shows some signs of life," he says. And AT&T has one big advantage on its side, he adds: "People are thirsty for multiuser microcomputers—and Unix is the only stuff out there." —Larry Waller

PRINTERS

ION-DEPOSITION PRINTER TAKES ON LASER

RANDOLPH, MASS.

Lasers most often are the technology of choice for nonimpact printing. But ion deposition is poised to make a big push into two bastions of the laser market—office automation and computer-aided design and manufacturing. That's the view of Delphax Systems of Randolph, Mass., which on Oct. 14 unveiled an ion-deposition system that for the first time combines text, graphics, a raster image processor, and printer controller all developed by Delphax—the company that holds the basic patents on ion-deposition printing.

Delphax, a seven-year-old company, had 1986 revenues of \$36 million, almost doubling from 1985. It supplies printers and print engines to original-equipment manufacturers, including Datagraphix, Honeywell, Northern Telecom, Olivetti, and Xerox. Now, with shipments of its S3000G RIP-equipped printer set to start in December, those OEMs could announce 30-page-per-minute combined text-and-graphics printers by early next year. The system holds special appeal in CAD/CAM applications, because it can print arcs and vectors much faster than plotters or dot-matrix printers.

Ion printing works by projecting ions onto a dielectric drum. The images attract a toner, which is then transferred to plain paper. It has become competitive with laser technology because it withstands duty cycles that are at least as high and often higher than laser printer duty cycles, according to CAP International Inc., a Marshfield, Mass., market-research firm that tracks the printer business. For example, the 30-ppm S3000G has a specified duty cycle of 225,000 pages per month; Thomas Kinney, Delphax's vice president for marketing, says Delphax OEMs will probably price the system between \$20,000 and \$25,000. Comparable laser printers' duty cycles are 35,000 to 60,000 pages per month, at 20 to 40 ppm, for \$15,000 to \$48,000.

For CAD/CAM, the S3000G will quickly print and collate unlimited multiple copies of engineering drawings and documentation. Today, those functions often involve a separate printer for drawings and documentation, plus time to

make multiple copies on a copier.

The heart of the graphics engine resides on a 14-by-16-in. board housed in a swing-out module on the back of the printer. The module also holds a 3½-in. floppy-disk drive and/or hard-disk drive.

New ion-deposition printers can do anything HP's LaserJet can do

An Intel 80286 microprocessor and 82786 graphics coprocessor make up the RIP, which provides all-points addressability plus various line-, arc-, and circle-drawing commands.

Standard electrical interfaces include Centronics and Dataproducts; Delphax will also design custom interfaces. Jeffrey Carrish, the company's director of product planning, says the floppy drive makes it easier to download new fonts or printer emulations than firmware systems.

The RIP feature is an important tool

in Delphax's diversification, says Catherine Dingman, associate director for nonimpact printing at CAP International. "They started as an engine company," Dingman says, "then progressed to providing full printers, mastering the paper-path problem. Now this puts them into controllers, and while printer suppliers can get a controller company to do that job, no one knows that ion print engine better than Delphax."

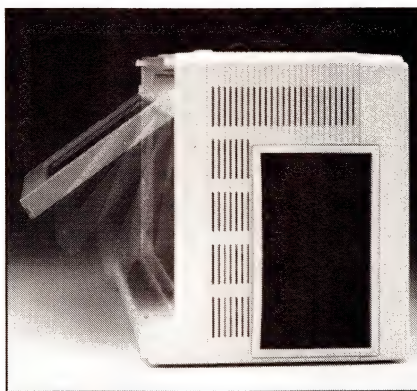
Delphax's Kinney points out that a substantial amount of printer software is being rewritten to run on networked systems—including Digital Equipment Corp. VAX systems and IBM Corp. 4341s—in market segments where nonimpact printing has yet to make significant inroads. "There are 25,000 sites where the average monthly print volume is somewhere between 100,000 to 500,000 pages," Kinney says. "Nonimpact printing has only 1% of that market, and less than 20% of the 7,500 sites where the volume is 500,000 to 2 million pages per month. Those are the markets that we're after." —Lawrence Curran

PORTABLE COMPUTERS

IT'S GETTING CROWDED FAST IN 80386 PORTABLES

SAN MATEO, CALIF.

The market for 80386-based portable computers is only a few weeks old, but already it's beginning to look like



SPINOFF. Dolch's 386 Pack portable is derived from an instrument controller.

Times Square on New Year's Eve. Almost every week, a new player has joined the fight, resulting in a three-way battle with more on the way. Latest to join is the king of the portables, Compaq Computer Corp., which came out with its model using Intel's speedy 32-bit microprocessor at the end of September.

Starting it all off was tiny Dolch American Instrument Inc. of San Jose, Calif., which introduced a 16-MHz machine originally developed as an instrument controller. A week or so later, Toshiba America Inc. of Irvine, Calif., announced its T5100, at 15 lb the lightest of them all, so far. And the Comdex show in Las Vegas, Nov. 2-6, should add to the crowd. Grid Systems Corp. of Fremont, Calif., for example, plans to introduce a pair of 286- and 386-based laptops.

"Portable" has always been a catch-all

term; early portables like Osborne's and Compaq's were "gut busters" that felt more like portable TV sets. Current models range all the way from 12-lb laptops to Compaq's 20-lb model. But whatever definition is used, the portable is fast becoming a giant market.

The strategy of Dolch and Toshiba was to beat Compaq to the punch and introduce 386-based computers that were the same size as the leader's 286-based Portable III [*Electronics*, March 6, 1987, p. 91] or smaller; they also were banking on higher performance and a lower price tag. In addition, Dolch hoped to gain an edge with more expansion capability than Compaq, and Toshiba with a more complete package—its T5100 has an integral EGA controller for higher-resolution graphics.

As it turned out, it didn't quite work that way. Not only did Compaq unveil its Portable 386 within weeks of the other two introductions, but the Houston company outflanked its new rivals in the performance contest. Instead of using the 16-MHz 80386, Compaq sprang a surprise by going to the advanced 20-MHz model.

Where the newcomers have an edge over Compaq is in price. Ken Pine, president of Dolch American, says the company's 386 Pack will sell for around \$6,495 with an installed 40-Mbyte hard-disk drive. The Toshiba T5100 machine, meanwhile, is priced at \$6,499. Compaq's Portable 386 costs \$7,999, but expansion is extra.

Volker Dolch, founder and president of Dolch American's holding company, Dolch Logic Instruments Inc. of San Jose, believes that the expansion capability of the 386 Pack makes it a more attractive portable than Compaq's. "With the Compaq machine, the user must add on an expansion module to the back of the computer," he says. "We built two full-width and two half-width expansion slots into the backplane."

The company derived this configuration from an instrument controller

called Cobra, for computer-based real-time analyzer, which was the mainframe for a set of configurable PC-based instruments. Instruments on a card—logic analyzer, waveform generator, and so on—can be plugged into the backplane to configure the system for a specific test function.

Toshiba designers don't think the user of a portable machine wants a large expansion capability. Thomas Scherrard, manager of PC marketing, lines up with Compaq in that regard. "When a user adds expansion cards such as a [local-area-network] card to a portable, it is no longer portable," Scherrard says. "It's a desktop system and can easily accommodate expansion via an external expansion chassis."

However, he feels that the portable does need some capability, especially EGA graphics, offered on an expansion card. So Toshiba has built an EGA controller onto its motherboard and designed the computer's gas-plasma display to accommodate the higher resolution, 640-by-400 pixels. The other two new machines have CGA as standard, for a resolution of 640 by 200 pixels.

To accommodate the user willing to sacrifice portability for expansion, the Toshiba unit comes with a single expansion slot, which can contain a 1,200-baud modem or an interface card that connects a five-card expansion chassis. The modem is built into the Compaq 386; a half-card modem can be added to the Dolch unit.

—Jonah McLeod

DIGITAL SIGNAL PROCESSORS

A NEW WAY TO GET FASTER, CHEAPER DSPs

FREIBURG, WEST GERMANY

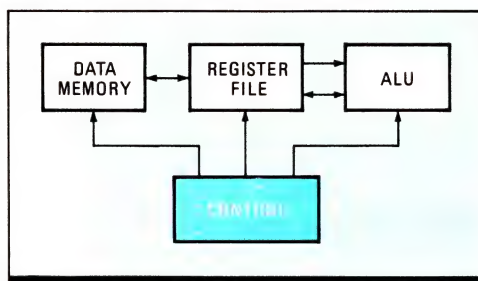
As digital signal processors find their way into more controller applications, DSP manufacturers are rushing to feed the trend with faster and less expensive parts. Now West Germany's Intermetall GmBh has come up with a new approach: a standard macrocell that is a microcontroller core for use with any of its DSPs. The design answers the high-speed, low-cost requirements of DSPs for TV and other consumer applications, and its new architecture could influence the design of DSPs for nonconsumer uses as well.

The controller is fast: 80 million operations/s. To get up to that speed, engineers at the Freiburg, West Germany, company used a mix of uncommon features even as they abandoned some principles, such as the use of interrupts, that long have been held essential in the data-processing community.

Beyond that, they held down the price by making the controller programmable, thus counteracting the rising cost of hardwired on-chip logic. And while most DSPs are primarily number crunchers for signals in the kilohertz range, with the new macrocell Intermetall's DSPs will crunch numbers in the megahertz range and also handle control functions.

Called the FP, for fast processor, the microcontroller will be fabricated in 1.5- μ m CMOS technology.

To keep real estate minimal, "we introduced reduced-instruction-set-computer ideas into the DSP architecture," says Martin Winterer, leader of the design team. The RISC features are single-cycle instructions and arithmetic operations performed entirely within the reg-



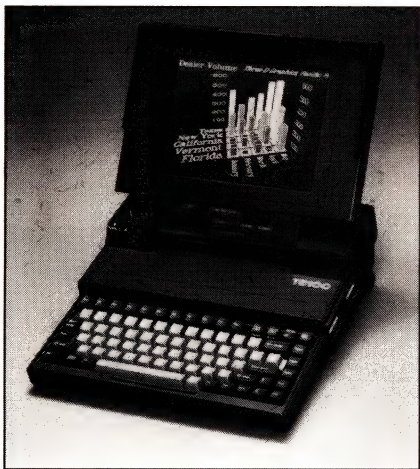
CONTROL BLOCKS. ITT's DSP controller core would consume only a fifth of the chip's real estate.

ister set with no need to access the data memory. The core also uses some design principles rarely combined in any chip: parallel processing, pipelining, multiplexing of the program ROM, and program scheduling.

Parallel processing gets around the "move" bottleneck of a Von Neumann design and doubles the data throughput. Achieving this is a controller core consisting of these blocks: the 128-byte data memory, register file, arithmetic logic unit, and control (housing the program ROM, typically 2 Kbytes).

BUSY UNIT. The register file can be read or written from both the RAM and the ALU. This keeps the ALU busy while input or output data is fetched or stored in parallel. Intermediate results can be stored in the register file, which holds eight 12-bit registers. The ALU performs additions, subtractions, and logic operations within a 25-ns cycle time.

The FP makes extensive use of pipelining so that operations that usually must be done serially can be performed in parallel. Processing an instruction is subdivided into individual units, each requiring a full clock period. Proper allo-



GRAPHICS. Toshiba's T5100 features an integral EGA controller for graphics.

cation of these units considerably increases throughput.

One unusual feature is the multiplexed ROM, which also helps boost the throughput. To keep memory bandwidth low, the FP fetches two instructions with each memory access and processes them one after the other, while fetching the next two. This complicates pipelining somewhat but does not affect the FP's functional behavior, Winterer says.

Significantly, the controller does away with interrupts in favor of program scheduling, "because interrupt schemes considerably interfere with high-speed processing requirements and call for lots of circuitry," Winterer says. Because the FP has no interrupts, it is markedly different from most microcontrollers. Usually, any controller must respond quickly to asynchronous demands. But with common interrupt

schemes, there is a need to restore the controller's internal state. With a register file, however, it either takes time to store and load all registers or it requires extra hardware to hold one or more additional file for context switching. Further, interrupting the pipeline and restoring it is a complex task, making extensive logic necessary.

So the Freiburg designers did away with interrupts, instead subdividing programs into individual tasks. While a task is running, no interrupt is allowed. When the task is completed, a hardware block, the so-called scheduler—part of the control block—decides which task must be executed next.

The scheduling scheme incorporated in the FP also supports a modular software structure, making the FP the ideal partner for fast controlling and signal-processing applications. —John Gosch

AVIONICS

HOW ABOUT THIS? AVIONICS WOULD GO IN PLANE'S SKIN

LOS ANGELES

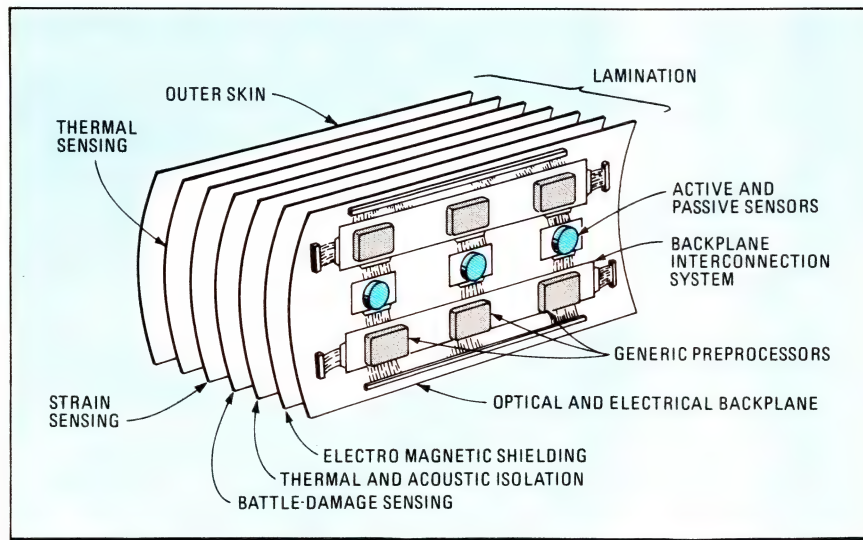
Here's a prediction for you: the military airplane of the future will carry its sensing, communications, and processing equipment embedded in its outer skin. At least, that's the conclusion emerging from a year of study by avionics and structural engineers at GMHE/Hughes Aircraft Co. and Rockwell International Corp.

The work was done as part of the Air Force's Forecast 2 project to identify new technologies for next-century equipment. The Hughes-Rockwell concept, "smartskins," envisions flexible electronic packages holding the various avionics subsystems, which would be

separated into layers and distributed over the body of the aircraft. The first usable embedded equipment could be ready in 5 to 10 years, the study says.

"This is a brand-new ballgame for avionics," says Joseph Smalanskas, laboratories engineer at Hughes, who is coordinating the two-year study. The goal is "nothing less than eliminating dedicated structures for electronics."

But first researchers have to overcome two tough technology barriers, says Smalanskas. The chief one is developing flexible optical-interconnect boards and backplane mounting to replace the rigid copper-based printed-circuit boards now in use. The boards must



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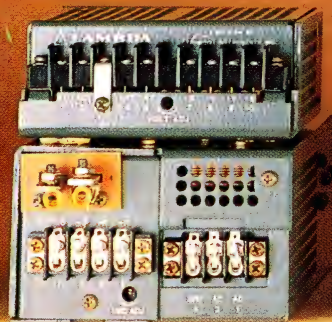
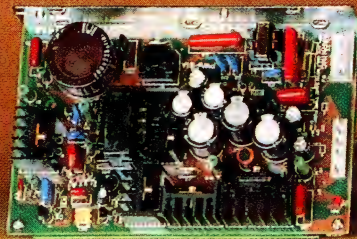
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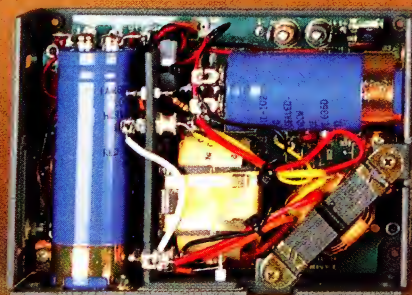
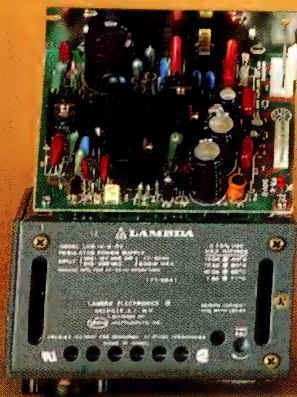
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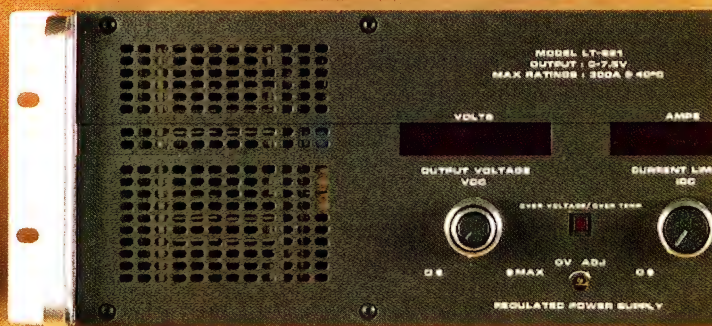
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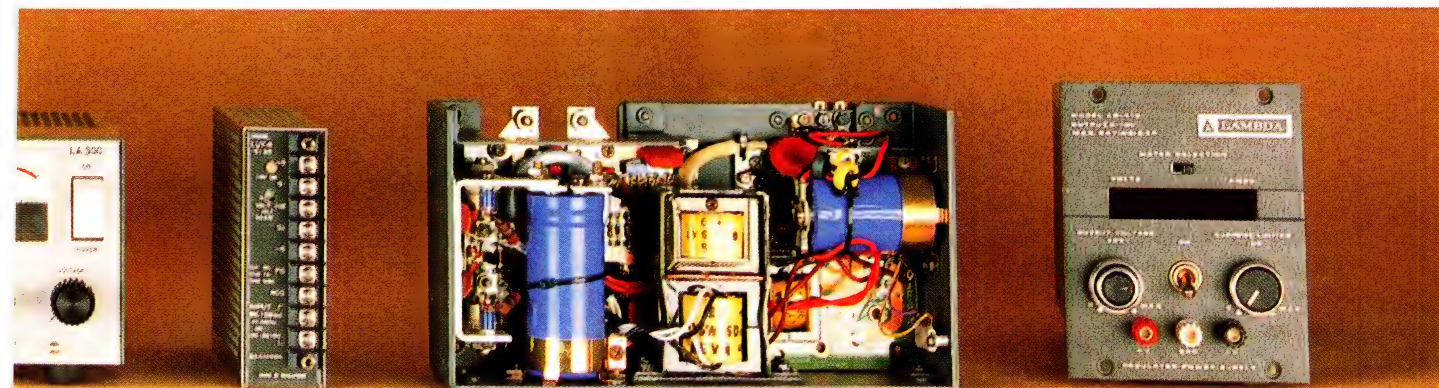
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be flexible so that they can be configured into shapes that fit into the surface of an airplane.

Also, localized cooling must be vastly improved and better heat-resistant materials developed, so that the electronics packages can survive skin temperatures that can reach 200°C. Part of the problem here is that semiconductor devices are getting so dense that power dissipation is up to 100 W/in.³.

The study stems from the Air Force's desire to get rid of the computer-crammed boxes that now carry avionics systems and that place limitations on both an aircraft and its electronics. For example, by distributing the processing power to the sensing or transmission sites, away from a central module, there are no interconnects to delay signals or to break down. Similarly, airplane designers could use the best aerodynamic configuration, free of processor boxes, sensing pods, and antennas.

The study concludes that smartskins would make for better maintenance, because the packages would be easier to reach than the boxes used now. And they would be more reliable, because

Electronics would be easier to maintain and weigh less, too

there would be fewer interconnects. A bonus is that weight could be cut 80% by replacing the copper that is used now in optical communications.

The underlying principle is central to any good design, explains Smalanskas: "fitting form to function." Some progress in that direction has already been made in the next-generation Advanced Tactical Fighter, now on the drawing boards for service in the mid-1990s, which combines formerly separate avi-

onics modules into a single rack.

The next major research task for the contract's second year will be to advance packaging and cooling technology, agree Smalanskas and his Rockwell counterpart, Angus R. Calder, technical staff member for advanced avionics. They believe advanced semiconductors for sensing and processing will come out of the Pentagon's Very High Speed Integrated Circuits program.

Once the study is completed, the Hughes-Rockwell team hopes to get a contract to build demonstration hardware for smartskins. At the Air Force Wright Aeronautical Laboratory in Dayton, Ohio, Air Force program manager Marvin Soraya says he is "waiting to see qualitative results" before giving an opinion. But, he adds, "the Air Force is very interested in smartskins, because many programs are tied to it. One thing is sure, avionics styles have to change, so the need is there." —Larry Waller

MEDICAL ELECTRONICS

NOW, A 3-D ROAD MAP FOR THE SURGEON

KIEL, WEST GERMANY

Computer tomography has become a basic diagnostic tool for surgeons, with the X-ray cross-sections of organ or bone providing a road map for operations. But a small West German company says CT leaves something to be desired—something that it can now provide.

MEK Medizinelektronik GmbH goes a step beyond CT, raising the conventional two-dimensional tomogram to the third dimension. Its Endoplan system processes the CT picture data and feeds it either to a screen to provide a 3-d image of the organ, or to a five-axis milling machine that produces a model, usually life-sized, from styrofoam or wax.

MEK will be the first to sell its system for use in hospitals. It will be available for \$250,000 to \$300,000 before the end of the year. A U.S. company, Cemax Inc.

of Santa Clara, Calif., already operates a similar system on its premises from scans sent by doctors and hospitals.

The technique has a number of advantages over 2-d imaging methods such as conventional radiography, CT, ultrasound, and magnetic-resonance imaging, says Ulrich G. Kliegis, one of MEK's two managing directors. The 3-d structure offers minute detail that leaves no doubt about the shape or other details of scanned organs or bony parts. Also, different medical personnel may interpret an organ's dimensions differently with a 2-d scan.

With Endoplan, surgeons can precisely and noninvasively pinpoint, for example, a tumor or a bone deficiency. From the patient's viewpoint, the more the surgeon knows, the more quickly the operation goes, says Kliegis, himself a physician. Also, the models can be used for trial bone surgery or for the automatic manufacture of prostheses.

A prototype has been undergoing tests at the University Clinique of Kiel since June. Doctors there are said to be enthusiastic, as are neurosurgeons, orthopedists, and plastic surgeons elsewhere who have heard about the system.

The Endoplan consists essentially of a Hewlett-Packard Co. HP320 work station, a MEK-designed picture-sequence memory, and the custom-made computer-driven

milling machine. A series of tomograms is made in which the structure to be modeled is recorded, with slice scans taken at the smallest possible intervals.

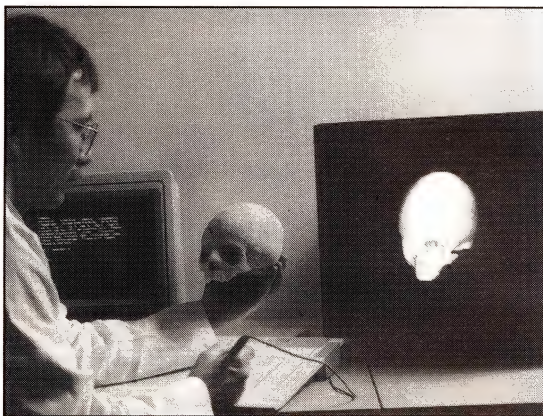
Next, the contours of the structure are found by following the lines of equal light intensity in the image plane. Here, the user can intervene in the contour-definition process and change the boundaries to separate adjacent or overlapping structures, such as are encountered in joints, for example. The detected contours, in the form of data, are stored by the work station.

After interpolating neighboring contours, a closed-surface representation is computed. Then the contours extracted from the slice scans are composed to form a 3-d model on a screen.

SCREEN BYPASS. The system can also bypass the screen and feed the data directly to the milling machine. With its five axes—two rotational and three linear—the machine automatically reproduces even complex structures like a human skull in all its details. It takes about eight hours from the time the tomograms are recorded to come up with a complex skull model, and very little, if any, human intervention is required. About 40,000 vectors, each containing a 25-byte set of coordinate data, are needed to produce the skull model.

Besides medical applications, MEK expects the Endoplan to also prove its mettle in industrial design—in making models of everything from shoes to engine blocks, says Wolfgang Schwesig, the managing director responsible for engineering.

—John Gosch



SKULL SESSION. Endoplan made this model of a four-year-old girl's skull in about eight hours using 40,000 vectors.

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PROBING THE NEWS

GaAs-ON-SILICON WAFERS ARE SET TO GO COMMERCIAL

WITH A DOZEN BETA SITES ALREADY, KOPIN CORP. WILL OFFER 4-in. WAFERS

by Lawrence Curran

TAUNTON, MASS.

Those chip makers eager to tap the high-performance potential of gallium arsenide should be more than a little excited about a brand new development in GaAs-on-silicon material: the commercial availability of 4-in. wafers, which are believed to be the first of their size to go on the market.

The source of these wafers, tiny Kopin Corp., was scheduled to disclose at this week's IEEE GaAs IC Symposium in Portland, Ore., that sample production had already begun on wafers measuring 2, 3, and 4 in. in diameter. Having the most potential is the 4-in. wafer, which will start shipping in December.

The marriage between GaAs and silicon [*Electronics*, Sept. 18, 1986, p. 31] is still tricky enough to prompt a wait-and-see attitude by some potential users, but the lure of joining the two materials to get the advantages of each—including the structural and thermal properties of a silicon substrate—is driving more than a dozen research efforts in the U.S. and Japan. GaAs emits light, withstands high temperatures, and survives high doses of radiation, making it attractive for optoelectronic and fast logic and memory devices, as well as for radiation-resistant integrated circuits. However, the brittleness and warping of bulk-GaAs wafers have so far limited diameters to 2 or 3 in. Also, GaAs often lacks purity when deposited on silicon.

Kopin is a three-year-old Taunton, Mass., startup that eventually will supply chip makers with production-quantity epitaxial wafers. The company has about a dozen beta-site customers for wafers, on which GaAs is grown using metallic-organic chemical-vapor deposition. John C. C. Fan, Kopin's founder, chairman, and chief executive officer, believes the commercial availability of these wafers represents "the enabling technology for future GaAs market growth."

That market has been frustrated until now, but it may indeed be stimulated by the promise of GaAs on sturdier, larger-diameter silicon-wafer substrates, promising the economies of scale associated

with silicon processing. Further, the ability to selectively grow GaAs on portions of a silicon wafer holds the potential to marry CMOS FETs with GaAs optoelectronic devices, including lasers. Texas Instruments Inc. is working on this kind of patterned deposition in its Central Research Laboratories in Dallas. So is GTE Laboratories Inc. in Waltham, Mass.

Wafer- or device-level programs are perking along with more than a dozen other entries in the GaAs-on-silicon sweepstakes in the U.S. and Japan. They include Fujitsu, Hitachi, Mitsubishi, NEC, NTT, Oki Electric, and Sharp in Japan, plus AT&T Bell Laboratories, Ford Microelectronics, Hewlett-Packard, and Spire in the U.S.

SPECIAL SILICON. There's not much that Fan wants to divulge about the way Kopin makes its wafers, but he does say that the company buys specially cut silicon wafers. "It is still 1-0-0 material, but it has a slightly different orientation," Fan says. That orientation, plus several processing steps, are intended to minimize defects and warping.

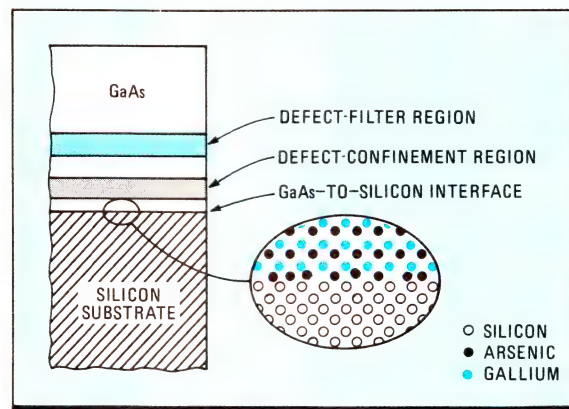
Kopin uses a proprietary cleaning process before putting the wafers into a modified chemical-vapor-deposition reactor. Two steps deposit a very thin "defect-confinement" layer before the GaAs is put down. The entire epilayer is a maximum of 8 μm thick, and usually

more like 5, Fan says. Thermal cycling follows to help take care of stress and lattice mismatches, says Fan.

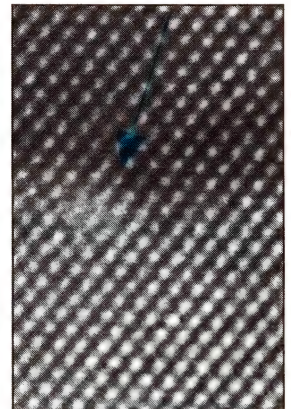
One of the biggest U.S. development efforts is at Texas Instruments Inc., where blanket deposition of GaAs across an entire wafer last year proved the quality of epitaxially grown GaAs on a passive silicon substrate. That work resulted in the most complex GaAs-on-silicon devices reported to date in the U.S.—fully functional 1-Kbit static random-access memories with address-access times as short as 6 ns [*Electronics*, Sept. 18, 1986, p. 31].

The thrust of TI's current effort is directed at patterned deposition, so that some circuit functions are done in GaAs and others in silicon. Its method is to grow GaAs through silicon-dioxide or silicon-nitride masks, a technique that "allows us to place single GaAs pads wherever we want on a silicon wafer," says Richard Matyi, a member of the technical staff in TI's Materials Science Laboratory. Hisashi Shichijo, senior member of the technical staff in the GaAs Logic and Memory Branch of TI's Central Research Laboratories, adds that the lab initially will use patterned deposition to combine silicon CMOS circuitry with GaAs MES FET circuits.

"Once you develop the technology to combine these two kinds of devices, you aren't limited to MES FETs or CMOS,"



LATTICE MISMATCH. Different lattice dimensions in silicon and GaAs result in interface dislocations (seen as a fuzzy spot in TI photo). Defects can propagate from them into the GaAs.



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Shichijo says. "You will be able to do biCMOS in silicon and combine that with GaAs." TI hopes to demonstrate patterned-deposition mixed-GaAs-silicon circuits as early as next year.

Development of such dual ICs is one goal of a five-year program at Ford Microelectronics Inc., Colorado Springs, Colo. Richard T. Habash, the company's business-development manager, says the other aim is to develop focal-plane arrays for radar applications. To do this, Ford employs metal-organic chemical-vapor deposition to grow GaAs-on-silicon wafers.

Habash says the company has built

TI and GTE are both working on patterned GaAs deposition

MES FETs in the GaAs layers that achieve about 80% of the performance of MES FETs fabricated in bulk-GaAs wafers. Next year, Ford will make its first attempt to grow GaAs on a silicon wafer already containing semiconductor devices.

The focal-plane-array work is aimed at fabricating optoelectronic ICs that can be used in Ford Aerospace radar systems in about three years. For these arrays, Ford first grows GaAs on a silicon wafer, then mercury cadmium telluride on top of the GaAs. Ford has grown those materials on both 3- and 6-in. wafers, "and we think we can do 8 in.," Habash says.

Optoelectronic ICs are also a goal of Oki Electric Industry Co.'s effort in Japan. But today's optoelectronic devices are playthings, says Katsuo Kaminishi, general manager of the Compound Semiconductor Device Laboratory in Hachioji. Oki wants to develop a material on which monolithic "hybrid" ICs bearing silicon and GaAs circuits as well as optical devices can be fabricated. It is also looking for ways of putting layers of other materials, such as indium phosphide, on silicon.

Kaminishi's group has used both molecular-beam epitaxy and the chemical-vapor-deposition process, but the current emphasis has shifted to the latter. He reports that the mobility of GaAs grown on silicon is high, resulting in FETs with essentially the same performance as those fabricated in bulk GaAs. But optical-device characteristics are not good yet, he says, probably because of higher defect densities.

Alfred Y. Cho, director of the Materials Processing Research Laboratory at AT&T Bell Laboratories, Murray Hill, N.J., has also achieved GaAs-on-silicon device performance comparable to that of GaAs-on-GaAs devices. Microwave FETs have been produced by ion implantation into molecular-beam epitaxially grown GaAs. A parallel effort at Bell Labs, using metal-organic chemical-vapor deposition, has

not been as successful yet, Cho reports.

Spire Corp., a Bedford, Mass., supplier of epitaxial wafers, has been working with GaAs-on-silicon chemical-vapor-deposition since 1982. Robert G. Wolfson, vice president for electronic materials, says the company holds the basic patent for the process. Spire recently got a \$50,000 contract from the U.S. Army's Electronics Technology and Device Laboratory, Ft. Monmouth, N.J., to develop techniques for 4-in. GaAs-on-silicon wafers.

"It looks like GaAs-on-silicon is almost as good as GaAs-on-GaAs for majority-carrier devices, such as FETs," says Wolfson. "But GaAs-on-silicon is definitely inferior for minority-carrier devices—lasers and solar cells." The principal obstacle is "threading," or the migration of defects from the interface into the GaAs region, Wolfson notes.

Researchers say that such defects are caused in large part by the different atomic lattice structures of GaAs and silicon: this creates dislocation defects at the interface between the two materials that can migrate far enough into the GaAs to degrade devices. However, Kopin's Fan says that initial reports from beta sites indicate that other results of growing GaAs on silicon—defect density and warping—may not be such serious problems as previously thought.

Indeed, one Kopin beta-site customer is pleased with the mechanical properties of the first wafers that he's seen. Richard Koyama, vice president of research at Triquint Semiconductor Inc., a GaAs IC-maker, says that the Beaverton, Ore., company has handled 3-in. Kopin wafers, "and they survived many of our processing steps. We were afraid that the GaAs epilayer would just peel off—and that hasn't happened."

At one point, Oki tried to minimize micro defects by depositing germanium and other superlattice layers between the silicon and the GaAs. But the company's current work eliminates any intermediate layer, substituting a two-step process in which GaAs is grown at a low temperature followed by a second, higher-temperature GaAs growth. (Kopin has likewise abandoned germanium.)

GTE Laboratories uses an intermediate layer, along with chemical trenching, to combat defects and warping. Leslie A. Riseberg, director of the lab's Electronics and Photonics Laboratory, says a superlattice buffer region—alternate layers of GaAs and AlGaAs—causes micro defects to propagate laterally rather than vertically, minimizing their migration into the GaAs active regions. Chemical trenching to relieve stresses nicely takes care of warping, he reports.

Additional reporting by Charles L. Cohen, Wesley R. Iversen, and J. Robert Lineback

We're growing with speed and resolution.



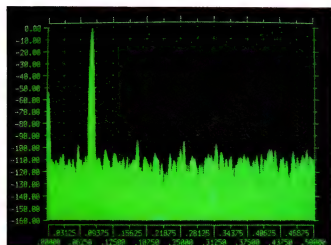
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Step-by-step, Analog Solutions is covering all key points on the speed/resolution scale.

We already have the largest line of high performance 16-bit ADC's. Now, in response to customer needs, Analog Solutions is introducing significant new products in a growing family of sampling A/D converters.

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Actual spectral performance of ZAD2846

Equally impressive is the ZAD2846, a 300 kHz sampling 16-bit ADC with the best linearity and lowest noise and harmonic distortion available. With its low drift and guaranteed specs, the ZAD2846 satisfies the most demanding applications. The FFT diagram shows the actual performance.

Both new products use the latest technology and Analog Solutions' proprietary digital correction sub-ranging architecture.

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Circle 49 on reader service card

YOU'RE ON AS YOUR

When you're trying to build the hottest new products you can think of, you need the latest, most sophisticated ASICs available. And the greatest number of ways to use them.

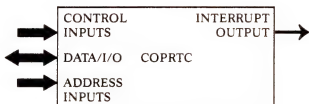
And that's the whole idea behind our Triple Technology.[™] Which gives you the ability to combine analog, digital, and E² cells all on the same chip. And the confidence that they all f

SEPTEMBER

Real-time Clock for COP[™] 800 Microcontroller Core

Key Features:

- Parallel interface to Sierra core cell
- Low power/independent operation
- Programmable interrupt system
- In-cell 32 KHz micropower crystal oscillator
- Timekeeping from 1/10 sec. to years
- Available in Sierra's 2-micron CMOS standard cell library.



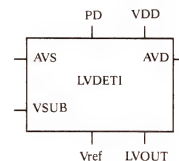
The COPRTC Real-time Clock peripheral has a direct interface to the COP800. It's 32 KHz crystal oscillator allows independent operation while the controller core cell is in a low-power halt state. The interrupt timer can "wake up" the controller at user-programmable intervals. This peripheral keeps time with tenth-second resolution and includes an automatic leap year calculation. Of course, it is also fully compatible with all the digital and analog cells in our Triple Technology[™] 2 micron CMOS cell library.

OCTOBER

LVDET1 Low Voltage Detector

Key Features:

PARAMETER	Min	Typical	Max	Units
Supply Range	2.5	5.0	5.5	Volts
Negative going trip point, V_{tr-}	3.7			Volts
Positive going trip point, V_{tr+}			4.5	Volts
Hysteresis $(V_{tr+}) - (V_{tr-})$	200			mV



This cell can be used to detect low battery voltage. Or to power down an electronic system safely in case of power interruptions, then reset it when power is restored. In either case, when power supply voltage drops below a specified value, this precision circuit provides a logic output. With built-in hysteresis and inherent low-pass filtering, it is immune to errors caused by small supply variations and spikes. It is also a perfect example of our commitment to introduce a new high-performance cell every month throughout 1987. Watch this space for November's cell.

LYAS GOOD LAST IDEA.

together, since they've all come from the same source. Of course, we already give you the best cell library in the industry. But every month this year, we'll use this space to introduce

our latest ideas. To give you more possibilities than ever. If you'd like to see our complete library card, just write or call. In the meantime, just look what we've done for you lately.

NOVEMBER

DECEMBER



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Circle 51 on reader service card



**Light stable,
flame retardant
plastics?**

**Take a tip
from Nixdorf:
Talk to Bayer.**



Type 8812 computerized cash register keyboard and line display housing made of Bayblend

If you're looking for the right material, why not do as Nixdorf's design engineering department did: talk to Bayer!

For the cabinet and keyboard of their type 8812 computerized cash register, Nixdorf now use the PC/ABS blend Bayblend. This is a thermoplastic noted for its outstanding light stability, good flame retardance and high heat resistance.

Bayer has one of the world's biggest ranges of high-performance engineering plastics:

®Apec (PAR), ®Bayblend (PC + ABS),
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®Desmopan (TPUR), ®Durethan (PA 6, PA 66), ®Leguval (UP), ®Lekutherm (EP), ®Makroblend (PC blends),
®Makrofol (PC film), ®Makrolon (PC),
®Novodur (ABS), ®Petlon (PET),
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Circle 179 on reader service card

INTERNATIONAL NEWSLETTER

JAPANESE HONE COLOR LCDs FOR LAPTOP PCs BY SELLING TINY TVs

Japanese electronics manufacturers are sneaking up on the 9-in. size needed to put active-matrix color liquid-crystal displays into laptop computers, by paying for the development effort through sales of "pocket" TV sets with smaller screens. A 5-in. active-matrix color LCD is allowing Hitachi Ltd. to set a size record with its first TV product in this category, which will sell for \$647, starting in December. Sharp Corp. chose a more moderate 3-in. size for its first product, scheduled for arrival October 15 at only \$339. Both companies use amorphous-silicon thin-film transistors for the active matrix and a backlight for a bright picture. Hitachi's screen has 115,200 dots in a matrix of 240 by 480 dots; Sharp's 240-by-384 matrix has 92,160 dots. □

GERMANY AIMS TO DEREGULATE PARTS OF ITS COMMUNICATIONS SYSTEM

After years of exhaustive and often heated discussions in government, industry, and academe, the West German government is getting set to adopt a package of proposals that liberalize—if only moderately—its communications sector. When this happens—the best guess is starting in 1990—private companies will be free to compete in some markets now controlled by the Bundespost communications authority. A draft Bundespost proposal outlining major restructuring through a policy of gradual change should be ready for submission to parliament early next year. Broadly speaking, it recommends that the Bundespost retain its monopoly on the telephone network, while the supply of terminal equipment for that network and value-added services that use it are opened to competition. It also suggests a reduction of tariffs, now among the world's highest, for business lines leased from the Bundespost. Parliamentary debate begins next year. □

UK MERGER WILL CREATE WORLD'S NO. 8 TELECOM MAKER

The European telecommunications industry is beginning to coalesce into large entities with worldwide clout. More evidence of this trend is the announcement by two UK companies, the Plessey Co. plc and the General Electric Co. plc, that they will combine their telecom subsidiaries in a 50-50 joint-venture company. When merged, Plessey Telecommunications & Office Systems Ltd. and GEC Telecommunications Ltd. will have annual sales of £1.2 billion and assets of £600 million, resulting in the eighth-largest telecom company in the world. The new company will sell transmission equipment, data-communications gear, and private-branch and central-office telephone exchanges, among other products. Plessey and GEC have been holding talks for some five years, but most analysts expected any merger to cover only System X operations, an area in which the two companies already cooperate. (System X is the digital central-office switch developed as a standard for use in the UK.) In other markets, they both compete with and complement one another: much negotiation remains before the details are worked out. □

HITACHI RECOMMITTS TO AN IBM-COMPATIBLE COMPUTER STRATEGY

Hitachi Ltd., like Fujitsu Ltd., is increasing its dependence on computers that use IBM System/370-compatible software, despite the high price IBM Corp. is extracting [*Electronics*, Oct. 1, 1987, p. 40]. Hitachi will deliver in March its new M-630 and M-640 small- and medium-size systems, which cover the performance range of IBM's 9370 model 20 through the 4381 in eight models. Both Hitachi machines have central processing units squeezed onto a single circuit board to improve price-performance. To do this, the M-630 features 52,000-gate custom logic chips fabricated in 1.3- μ m CMOS; the M-640 does it with 5,000-gate emitter-coupled-logic devices. □

INTERNATIONAL WEEK

CASIO ENTERS DAT AND VCR MARKETS

Casio Computer Co., Tokyo, a leading manufacturer of calculators, watches, and liquid-crystal-display color TVs, is diversifying into the digital-audio-tape recorder and portable video-cassette recorder markets. It will start selling its 148,000-yen portable DAT, DGZY1, in December, about the same time as Matsushita and Sony go to market with theirs. The initial production rate will be 1,000 units a month. The portable VCR, VF-3000, has a built-in 3.3-in. liquid-crystal TV that can reproduce color images on its 118,580-dot display and receive off-the-air TV programs. Casio will start marketing the VF-3000 in mid-December at 125,000 yen with another 27,000 yen for accessories, initially producing 3,000 units a month.

TOSHIBA TO SELL 3-D CAMCORDER

Toshiba Corp., Tokyo, has developed 3D-CAM, the world's first camcorder capable of recording three-dimensional color pictures that can be played back on conventional VHS-format VCRs and a monitor with double scanning speed. Liquid-crystal-shutter glasses are required to view the 3-d images and a special adapter unit is needed for playback on standard VCRs. Toshiba will sell the camcorder for industrial as well as home use. It has not yet decided when to begin marketing the 3D-CAM, but it expects to price it at around 300,000 yen, 50% higher than the price of standard camcorders.

GERMANS GET FAST FIBER-OPTICS LINK

West Germany's Siemens AG has turned over to the Bundespost, the communications authority, the country's first fiber-optic line operating at a 565-Mbit/s data rate.

With 32 glass fibers in a cable spanning the 100 miles from Munich to Nuremberg, the link will have a capacity for 120,000 telephone channels or 64 TV channels, each with a 140-Mbit/s rate. The use of monomode fibers allows a repeater spacing as wide as 35 km.

FINNS, SWEDES GET VIDEOPHONE LINK

Finns and Swedes can now make videophone calls as easily as ordinary telephone calls. The first international videophone call was made from Helsinki to Stockholm on Sept. 24, using a digital link between the two national switched 64-Kbit/s networks. The videophones were made by Vistacom Industries Inc., a new Finnish company that makes color video codecs and terminals for 64-Kbit/s networks. Called Diginet, the switched 64-Kbit/s service is compatible with the Integrated Services Digital Network, with which it competes, and is supported by Nokia, Ericsson, and Siemens.

TURKS BUY SIEMENS DIGITAL SWITCHES

Turkey has become the 30th country to order an EWSD digital switch from Siemens AG, Munich. The order initially is for nine systems, capable of handling a total of 100,000 subscriber lines, to be used in eight cities throughout the country. Starting in 1988, the Turks will build EWSD systems on their own in a factory for which about \$23 million has been earmarked by the Ankara government.

PLESSEY, TELENET IN DATACOM VENTURE

The Plessey Co. plc and Telenet Communications Corp., a US Sprint company in Reston, Va., have formed a joint venture company, Plessey-Telenet Ltd., to market data-communications and packet-

switched networks and systems, initially in the UK and Holland. Ownership of Plessey-Telenet, which will be based at Basingstoke, England, is 51% Plessey, 49% Telenet. Plessey-Telenet already has orders valued at £30 million with ongoing contracts for private packet-switched networks.

VENEZUELA TO BUY ERICSSON SYSTEM

Ericsson Radio Systems of Stockholm, Sweden, has received a letter of intent from the Venezuelan Telephone Administration for a cellular mobile telephone system initially valued at \$12 million. The system will consist of one AXE mobile telephone switch and 10 radio base stations. Venezuela will be the first Latin American country to operate a fully automatic cellular service, the first phase of which will be installed in the Caracas area.

ARIANESPACE HAS EDGE OVER NASA

Now that its Ariane V19 booster has placed a dual payload into transfer orbits, Arianespace says it has received 44 contracts running into 1991 for launching satellites. The orders, worth \$2.38 billion, include nine U.S. private satellites. The consortium has offered to launch Indonesia's Palapa B-2R telecommunications satellite earlier and at a price 10% less than that of a U.S. Delta rocket launching, but a contract has not yet been signed.

PHILIPS, FLUKE PACT IS SET

Philips Test & Measurement of Eindhoven, the Netherlands, and John Fluke Manufacturing Co. of Everett, Wash., have set the terms of their March agreement [*Electronics*, April 2, 1987, p. 55]. Fluke will sell, service, and support Philips's products in North America, China, Hong

Kong, and Japan, while Philips will reciprocate for Fluke's products in the rest of the world. The accord also provides for technology transfer and joint product development.

ALCATEL LANDS TWO VIDEOTEXT ORDERS

Alcatel NV received two large orders in September to make videotext systems similar to the French Minitel for the Centre d'Excellence en Télécommunications Intégrées in Montreal and for Encode International in Houston. The Canadian contract calls for 100,000 terminals during the next 14 months and another 100,000 per year for the next five years. The contract with Encode calls for an initial 12,000 videotext terminals, with orders for 5,000 to 10,000 per month to follow.

UNIX-BASED MICROS COMING FROM BULL

France's Groupe Bull is making a play for the small-to-medium-size business-computer market in most of Western Europe, which it expects to reach 12.5 billion francs soon, with Unix-based super microcomputers in the Questar 700 family. The Bull Questar 700/15, 700/20, and 700/30 are being offered in compact frames for unit prices ranging from 140,000 to 210,000 French francs.

UK BOOK-TO-BILL SLIPS BELOW ONE

The UK book-to-bill ratio for electronic components in August fell below parity at 0.94 for the first time since November 1986, says the Electronic Components Industry Federation. Despite the low figure, which is typical of ratios in the second half of the year, sales continue to show slow, steady growth. Demand in consumer electronics was strong, the ECIF says, but defense was sluggish.

INTERNATIONAL PRODUCTS

TWO CHIPS DO ALL THE DECODING FOR AUTO COMPACT-DISK PLAYER

PHILIPS'S 1.5-MICRON CMOS CHIPS CUT POWER CONSUMPTION BY 83%

Designers of automobile stereo sound systems and other applications where high integration and low power dissipation are important can implement a complete stereo decoding system for compact-disk players with Philips's two-chip set and a few components.

By using 1.5- μ m CMOS technology, the Dutch company reduces power consumption to one sixth that of the company's previous generation four-chip set, which was fabricated in n-MOS technology. The SAA7310 and SAA7320 CMOS parts consume 475 mW compared to 3 W for the n-MOS chips.

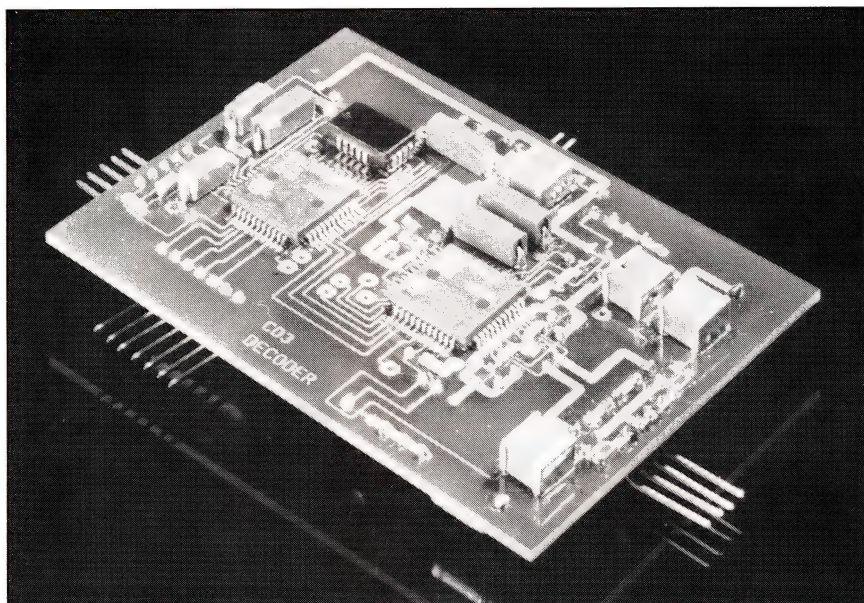
5-VOLT SUPPLY. The low power requirement means that the entire decoding system can operate from a single +5-V supply, says David Slowgrove, marketing engineer for the two circuits at the Philips affiliate Mullard Ltd. in Southampton, England.

Besides offering advantages over Philips's previous generation of CD decoding ICs, the SAA7310 and SAA7320 also outperform solutions from Far Eastern competitors. Other sets depend on peripheral devices to do part of the filtering, for example, but this job is performed on-chip by Philips's set. Still another plus is a wider operating temperature range—from -40°C to +85°C compared with -20°C to +70°C for Philips's earlier four-chip set and for competitors. The wider range is important especially in automobile applications.

For the two-chip decoding set, Slowgrove sees a big demand ahead, spurred by the steeply rising sales of compact-disk players around the world. Experts predict global purchases of between 10 and 15 million such players this year. For 1988, the forecast is for 20 to 25 million units, and in 1989 the number should top 30 million.

"We are hoping for a 20% to 25% share of the market," Slowgrove says. He adds that the stereo decoder set is aimed primarily at the midrange market—portable players and in-car systems.

The 7310 handles the same decoding functions—demodulation, error correction, and basic interpolation—as the previous-generation SAA7210. But it also



COMPLETE. Philips's two-chip set—packaged in 44-pin flat packs—integrates most functions of a CD stereo-decoding system, including filtering, which is implemented in three phases.

offers expanded features, including a special mode for nondigital audio applications. This function is particularly useful in CD read-only memory and interactive CD systems where the disk simply stores text data and still photos, because it prevents data from being interpolated—and corrupted. The 7310 is also designed for improved playability (compared to the 7210) in applications where mechanical shock is likely to occur, such as portable and in-car systems.

The other circuit, the 7320, handles digital filtering, over-sampling, and post-analog filtering.

FILTERING. For post-analog filtering, the 7320 has two operational amplifiers per channel, an implementation that requires only a few discrete components in its periphery. The circuit also performs muting, deemphasis and -12 dB attenuation functions. A second-order noise shaper makes for a signal-to-noise ratio of greater than 90 dB.

The 7320 takes the concept of over-sampling to the limit, achieving 16-bit resolution at 44.1 KHz by using one-bit digital-to-analog conversion at an 11.2-MHz sampling rate.

Three stages of digital filtering are implemented to provide the over-sampling multiplying factor of 256 required for one-bit digital-to-analog conversion. The first stage uses a 128-tap finite-duration impulse-response filter to achieve a four times increase in over-sampling. The filter also provides improved low-pass filtering compared to the 7220 of Philips's earlier four-chip set, which has a 120-tap FIR.

The second stage further increases over-sampling by a factor of 32 thanks to the use of a linear interpolator. Finally, a sample-and-hold circuit doubles the over-sampling to give the required 11.2-MHz data rate.

Following the digital filter stages is a conversion circuit that changes the data rate to a one-bit code and handles the actual digital-to-analog conversion. Conversion is by using a switched-capacitor technique. A fixed charge is either added or subtracted from the virtual earth node of a first-order filter.

This scheme provides greater linearity than a conventional digital-to-analog converter. Since there is only one converter stage involved, there's less de-

pendence on component tolerances.

Data exchange between the 7310 and 7320 is over the Philips I²S (for inter-IC signal) bus. This three-line bus dedicates one line each for the clock, serial data, and control data. Since I²S was also used in the Philips second-generation set, a combination of second- and third-generation devices can be used in the same system.

The 7310 and 7320 are both available in a 44-pin quad flatpack. The 7310 can also be had in a 40-pin dual in-line package which can be used as a replacement for the 7210 of the second-generation set. Samples of the two devices will be available in the fourth quarter.

Prices for the two circuits depend on importing country and local market demand. However, as an indication of approximate prices, the SAA7310 costs around 36 Dutch guilders apiece in 1,000-lot quantities and the SAA7320 about 40 Dutch guilders apiece, also in 1,000-lot quantities.

— John Gosch

Philips Elcoma, P. O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone 31-40-722091 [Circle 500]

SPECTRUM ANALYZER STORES 128 KBYTES

The MS2601A spectrum analyzer handles signals ranging from 10 KHz to 2.2 GHz and is the first in Anritsu Corp.'s product line to offer plug-in memory cards that provide up to 128 Kbytes memory for storing measurement parameters and traced data.

Microprocessor control ensures measuring accuracy to 1 dB in a dynamic range of 75 dB. The MS2601A also offers ease-of-use features such as zone markers—to locate signal peaks—screen scroll, and a frequency counter.

Applications include frequency and impedance measurements, electromagnetic interference analysis, and network analysis. The MS2601A is available now. Price depends on importing country.

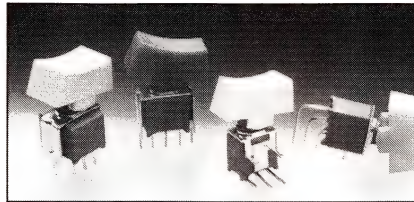
Anritsu Corp., 5-10-27, Minami Azabu, Minato-ku, Tokyo, Japan 102, Japan.
Phone 81-3-446-1111 [Circle 701]

SWITCHES SHRUG OFF SOLDER CLEANING

The TR series of sealed subminiature switches from MORS Composants can be soldered and cleaned on printed-circuit boards without danger of malfunction due to contamination.

Their small size—9.1-by-8.1-by-7.1 mm—means they take up minimal space on a pc board. They feature a rocker actuator and come with gold- or silver-plated contacts.

The two-position versions have a projected operating life of 60,000 operations



and the three-position versions have a projected life of 30,000 operations.

Available now in a variety of colors, export pricing for the TR series of mini-switches range from \$1.25 to \$2.50 each in volume purchases.

MORS Composants, BP No. 1, 82300 Caussade, France.

Phone 33-63-93-14-98 [Circle 702]

BACKPLANES INCLUDE TERMINATION CIRCUITS

British Telecom's 4610 series of backplanes for the emerging STEbus industrial standard saves users £30 usually spent on separate termination modules by integrating all bus-termination circuitry into the board.

On-board termination circuitry is located between the connectors to minimize system size. The board's multilayer construction implements separate 5-V supply and ground planes, giving the boards high immunity to noise and crosstalk.

The backplanes are supplied populated with female DIN41612 connectors on a standard 0.8-in. pitch and cost £65 and £105 respectively for 5- and 10-slot versions. They are available now.

British Telecom, Microprocessors Systems Group, Martlesham Heath, Ipswich IP5 7RE, UK.

Phone 44-473-643-101 [Circle 703]

DAC BOASTS FAST SETTLING TIME

Ferranti Electronics Ltd.'s ZN599 8-bit digital-to-analog converter has a typical output voltage settling time of 1.25 µs and a gain temperature coefficient of 2 parts per million per centigrade degree.

Designed to provide complementary conversion functionality for the company's ZN449 analog-to-digital converter in microprocessor-based systems, its maximum linearity error is plus or minus the least significant bit and monotonicity is guaranteed over the commercial operating temperature range.

Available now, the DAC comes in 16-pin plastic or ceramic dual in-line packages and in the SO-16 package for surface mounting. The device costs £1.81 each in 100-unit quantities. Export price is \$2.98 U. S.

Ferranti Electronics Ltd., Fields New Road, Chadderton, Oldham, Lancashire OL9 8NP, UK.

Phone 44-61-624-0515 [Circle 706]

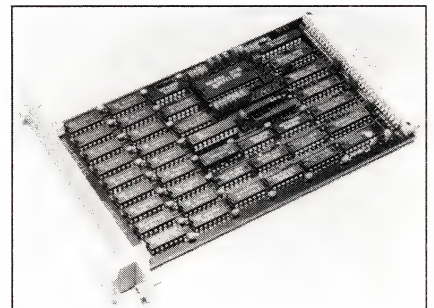
RAM CARD ALLOWS MEMORY-MAPPED I/O

The 512K8 dynamic random-access memory module from PEP Modular Computers GmbH implements memory-mapped input/output and has hidden refresh for the intelligent I/O channel. Its capacity extends from 64 Kbytes up to 512 Kbytes, with one-bit parity generation and check.

The module has 20 address lines for operation in the extended 1-Mbyte address range but may also be used in the basic 64-Kbyte address range. Within the address range, up to 16 blocks can be selected, allowing memory mapped I/O in the module's range.

The 512K8 may be used in synchronous or asynchronous bus systems. The asynchronous access improves data throughput and optimizes system speed. For synchronous operation, a bus frequency up to 2 MHz is available. The module has an access time of 250 ns.

For every written byte, one parity bit is generated and stored. This parity is com-



pared with the parity of the data byte during the read operation. A bus error signal is generated if the parity does not match. This allows detection of one-bit errors. The 512K8 module is available from stock for a price of 950 DM.

PEP Modular Computers GmbH, AM Klosterwald 4, D-8950 Kaufbeuren, West Germany.

Phone 49-8341-81001 [Circle 704]

PHILIPS HYBRIDS CUT NOISE 25%

The OM2000 wideband hybrid integrated circuit amplifiers from Philips offer noise figures about 25% less than existing equivalents in the Philips product line. The 12-V hybrid amplifiers, for room antenna, mast antenna, and community antenna TV systems, are aimed at wideband amplification in the range from 40 to 860 MHz.

Type numbers in the range are the OM2045, OM2050, OM2060, OM2061, and OM2070. The OM2045 has a gain of 12 dB with a noise figure of just 3.6 dB. The OM 2070 occupies the other end of the range and offers a 28 dB gain and a noise figure of 4.8 dB. Compact in design, the devices measure from 14-by-8

mm for the OM2045 to 27-by-22 mm for the OM2070.

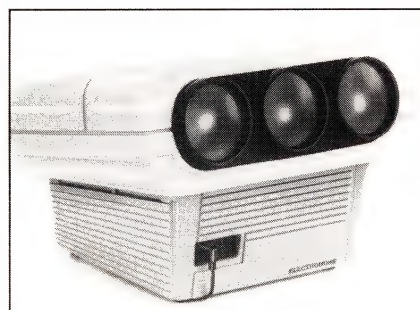
The hybrid amplifiers are implemented in thin-film technology. They have a source and load impedance of 75 Ω and an operating ambient temperature range from -20°C to +70°C.

Small quantities are available from stock. In 100-piece lots, the devices cost from 7 to 10 Dutch guilders apiece, although actual prices depend on type, order quantity, and importing country.

Philips Elcoma Div., P.O. Box 523, 5600 AM Eindhoven, The Netherlands.
Phone 31-40-757005 [Circle 707]

CAD DRAWINGS CAN BE SHOWN ON BIG SCREENS

Electrohome Ltd.'s ECP 3000 video projection system uses three-lens technology to deliver resolutions suitable for projecting computer-aided design drawings on 5-ft. to 25-ft diagonal screens.



The unit accepts inputs directly from video and high-resolution graphics terminals and has a memory capacity sufficient to store setups for 28 input parameters such as brightness, contrast, and convergence.

It automatically locks into horizontal scan rates of 15 to 50 KHz and offers 650 lumens peak light output. Horizontal retrace time is less than 4 μ s and vertical retrace is less than 300 μ s.

Available now, the ECP 3000 costs \$14,995 U.S.

Electrohome Ltd., 809 Wellington St. N., Kitchener, Ontario, Canada N2G 4J6.
Phone (519) 744-7111 [Circle 705]

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Heinzinger GmbH, P. O. Box 1076, D-8200 Rosenheim, West Germany.
Phone 49-8031-44040 [Circle 709]

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The CC-97 single-board computer from Compcontrol BV integrates the functionality of four separate boards in 16-bit VMEbus systems. It includes the processor; a Small Computer Systems Interface; 2 Mbytes dual-ported dynamic random-access memory; and 384 Kbytes of static RAM and erasable programmable read-only memory.

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Key chips on the board include a 16-MHz Motorola Corp. 68000 microprocessor and a Western Digital Corp. WD33C93 SCSI controller.

The board is available now. Export price is \$3,685 U.S. Price in the Netherlands is 7,250 Dutch guilders.

Compcontrol BV, Stratumseind 31, P. O. Box 193, 5600 AD, Eindhoven, The Netherlands.

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Miniature transformers in the OB (for on-board) series from Avel-Lindberg Ltd. offer a load-specification range of 0.8 to 30 VA and conform to eight international standards. The 0.8 VA version stands only 10.5 mm high.

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The 18-, 24-, and 30 VA versions can be mounted on boards with 1.5-in. spac-



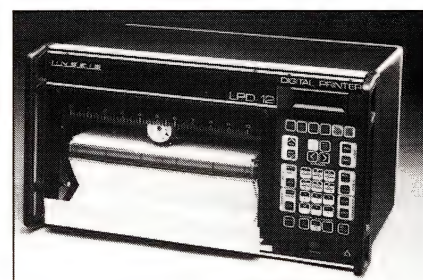
ing. Dual primary windings can be connected in parallel with 120-V ac and in series with 240-V ac power supplies. Nominal operating frequencies are 50 or 60 Hz.

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Linseis GmbH, P. O. Box 1404, D-8672 Selb, West Germany.

Phone 49-9287-79022 [Circle 711]

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Thomson Semiconducteurs, 45 Avenue de l'Europe, 78140 Vélizy-Villacoublay, France.

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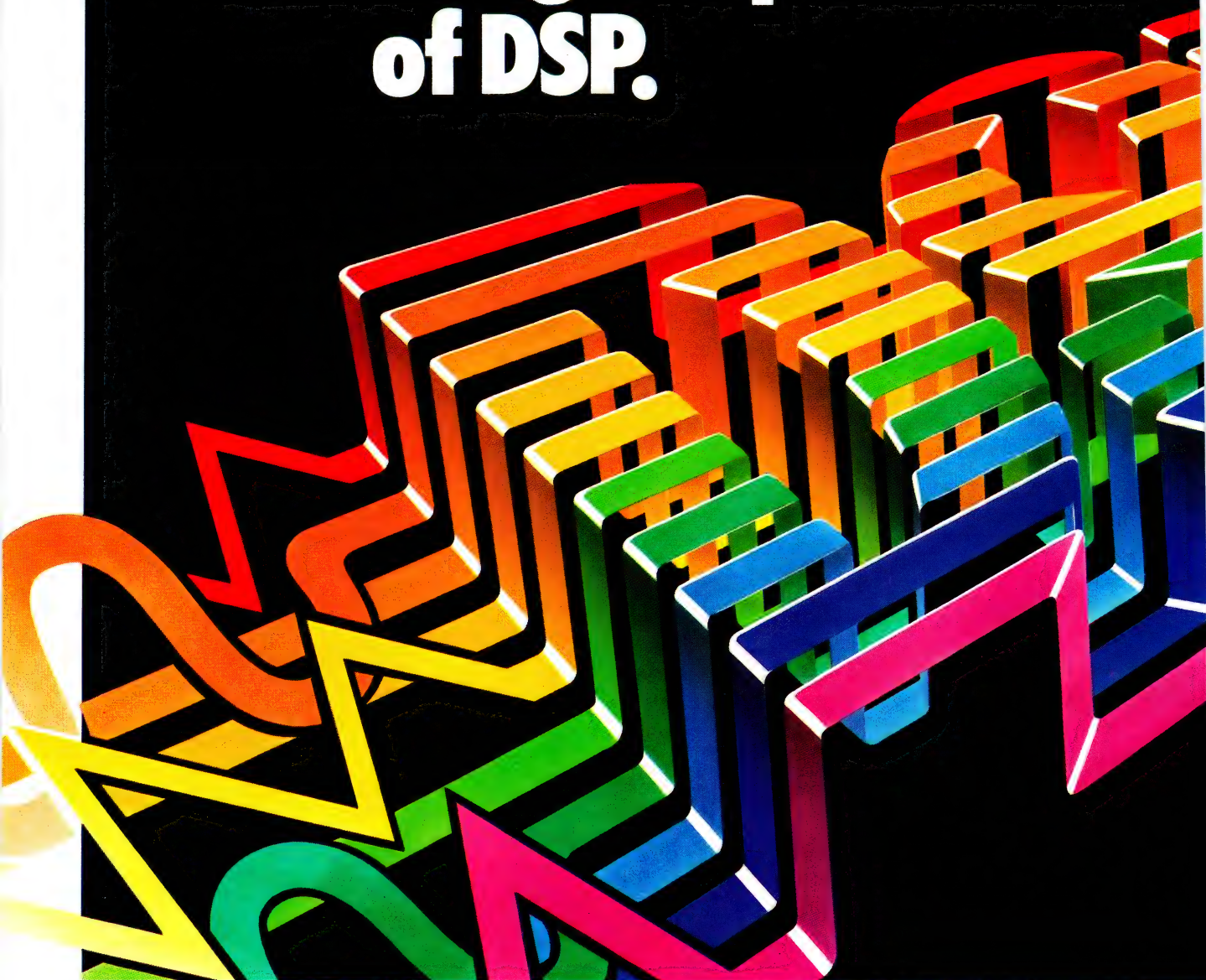
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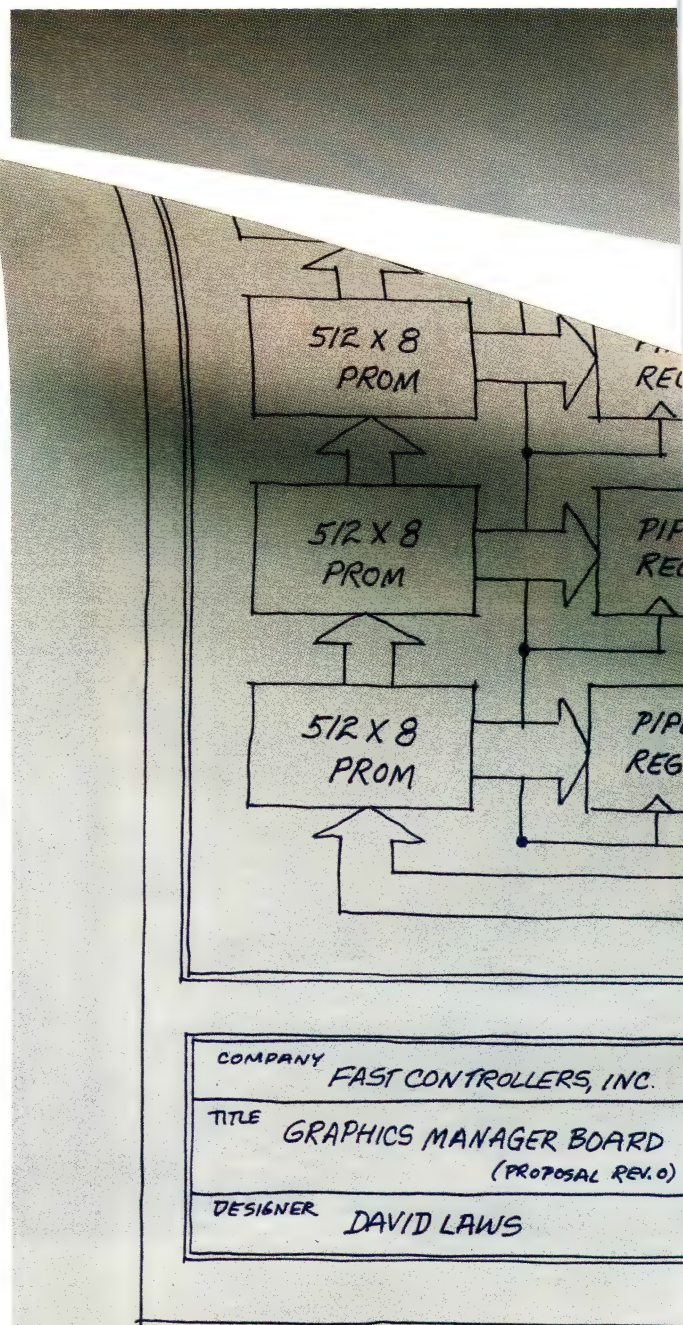
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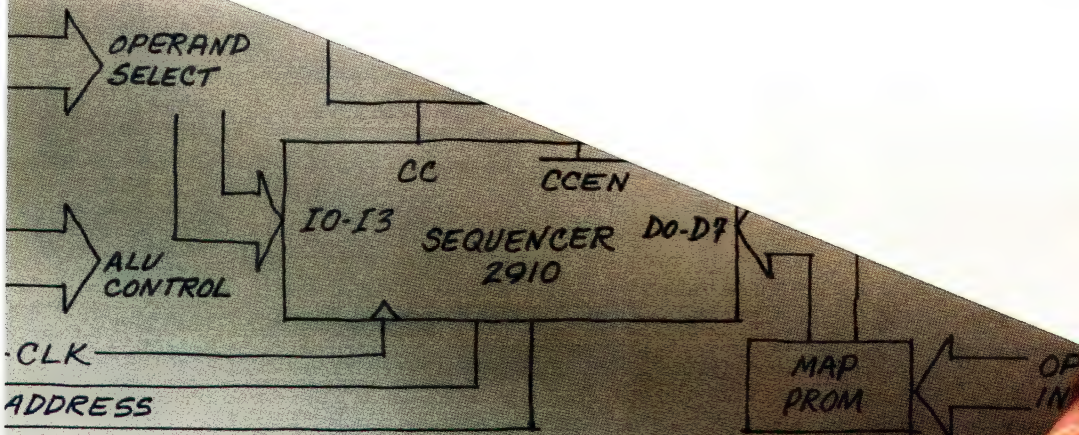
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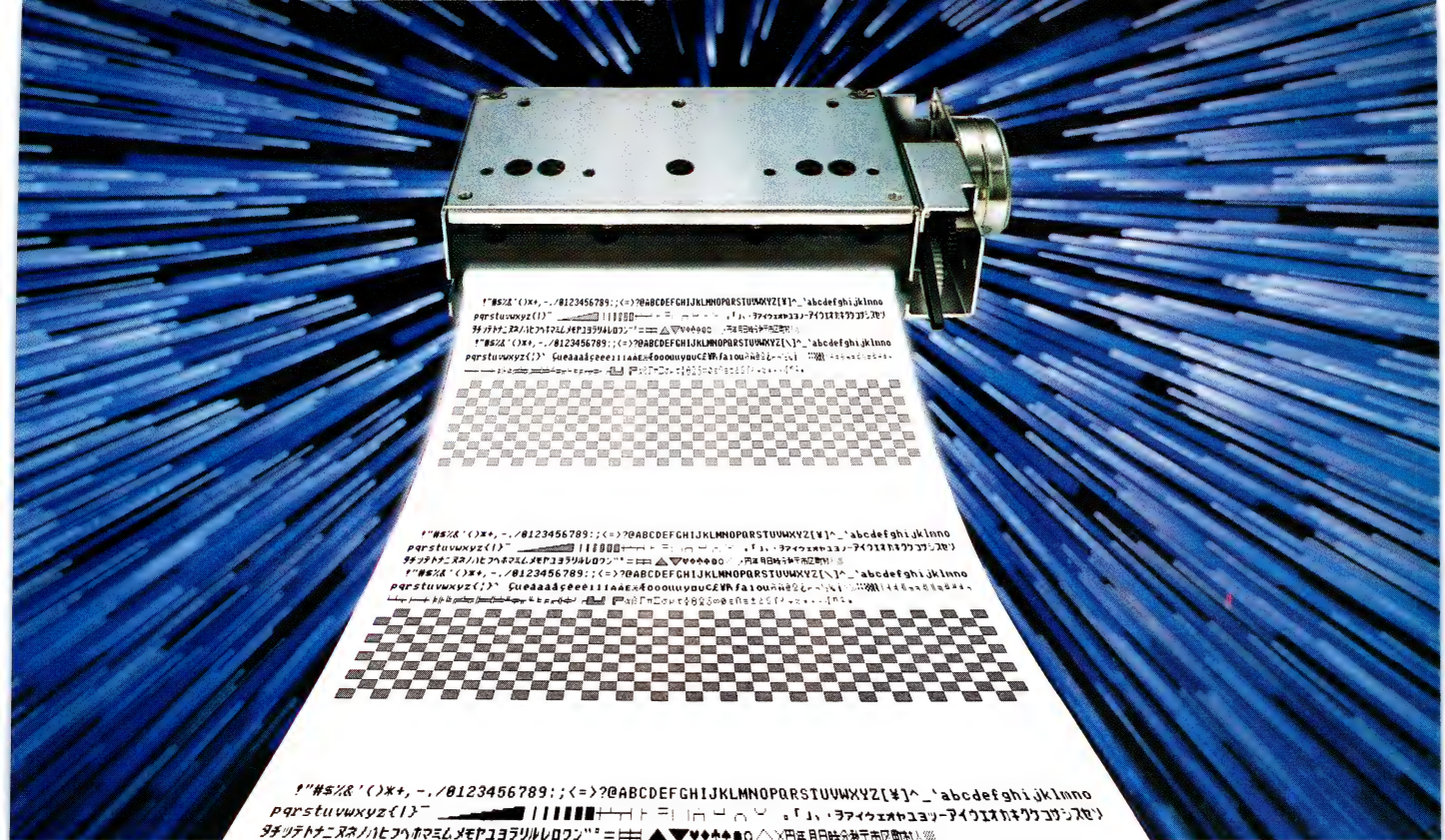
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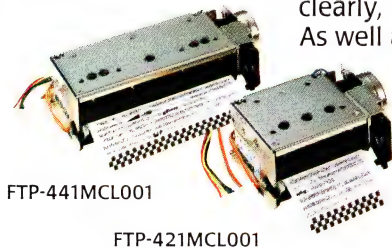


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Printing method	Thermal line dot	
Dot matrix	640 dots/line	320 dots/line
Effective print width	105.6 mm	52.8 mm
Horizontal dot pitch	0.165 mm (6 dots/mm)	
Printing speed	250 dot lines/s (at 25°C and 60% RH)	
Paper width	114 mm	60 mm
Exterior dimensions (W) × (H) × (D) mm	160 × 40 × 60	107 × 40 × 60
Weight	Approx. 600 g	Approx. 300 g

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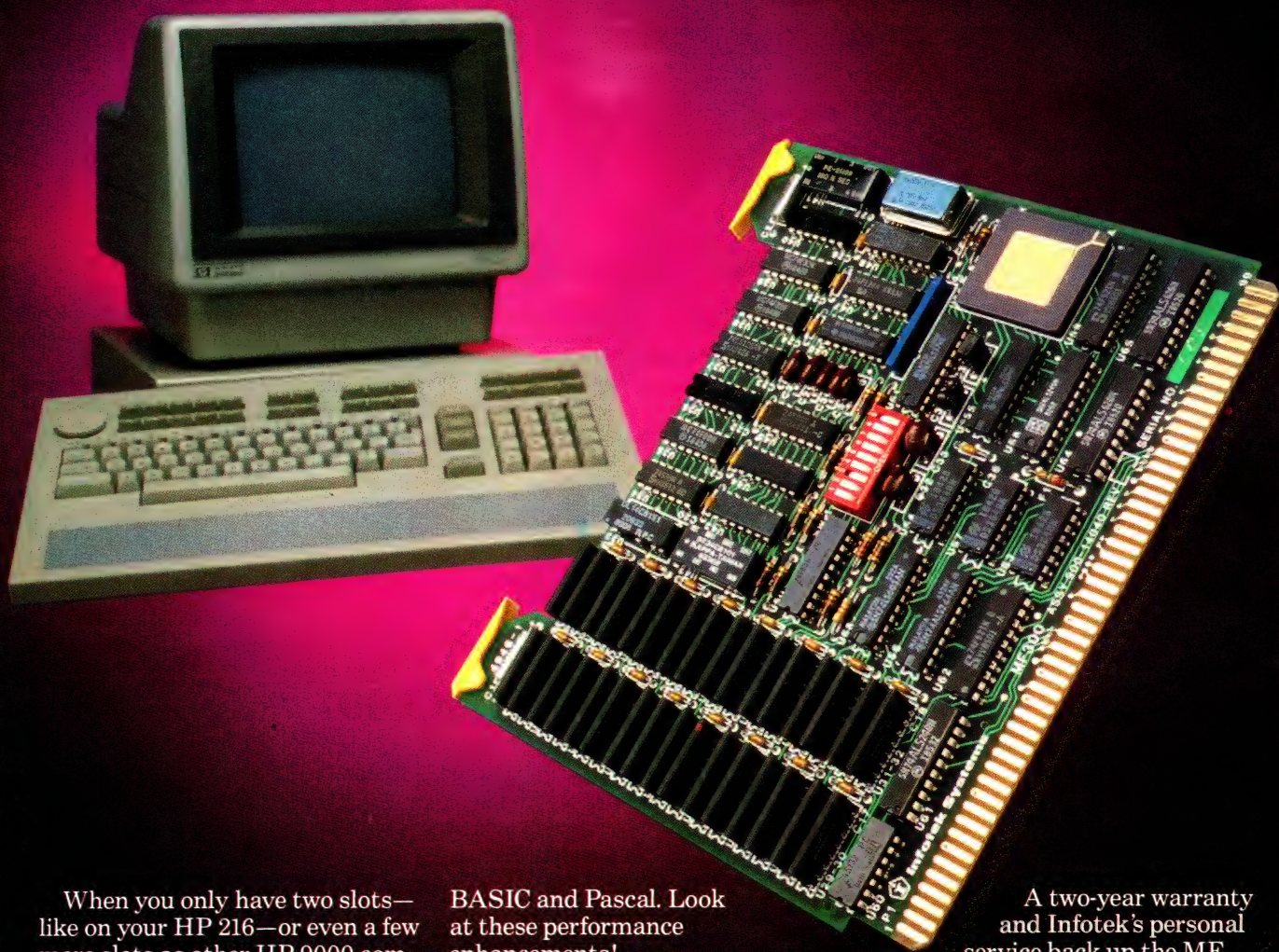
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Compiled BASIC

Statement	Computer	Without MF	With MF	Ratio
X=Y*Z	216	259	50	5.2
	310	161	37	4.2
X=SQRT(Y)	216	2,117	38	56
	310	1,333	30	44
X=SIN(Y)	216	4,326	64	68
	310	2,746	50	55

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INSIDE TECHNOLOGY

UNIX: LOOKING BETTER

The position of Unix as a world standard appears all but assured now. It has won the engineering and technical work-station market and looks like a strong candidate to capture a significant portion of high-performance personal computing. The promise of standards is the user's independence from a specific vendor's products—the customer's ability to pick and choose from a variety of applications software and hardware type, size, and cost.

A flurry of standards activities, some of it outside the realm of operating systems, is contributing to the health of Unix. The strongest sphere of support is from the major Western European computer makers (see p. 70), who have embraced it for all but their biggest mainframe systems. The only laggard is Japan, but Unix is making progress there, too (see p. 72).

Unix has clinched the technical work-station market with a whopping 83% share (see table, p. 68), and now it's spreading elsewhere. Growth in the Unix-system markets is expected to outstrip that of other computer environments during the next few years (see chart, below).

But this kind of growth will not occur without more help from the standards bodies. AT&T Co. has a certification process for compliance to its System V standard, but the industry wants control of the standard to rest outside any single company. Now the IEEE has come up with a fledgling draft standard for a programming interface, called Posix.

One of the most exciting developments is the

A big European push and agreement on interfaces move it closer to a worldwide standard; work stations have fallen in line and high-performance PCs are next

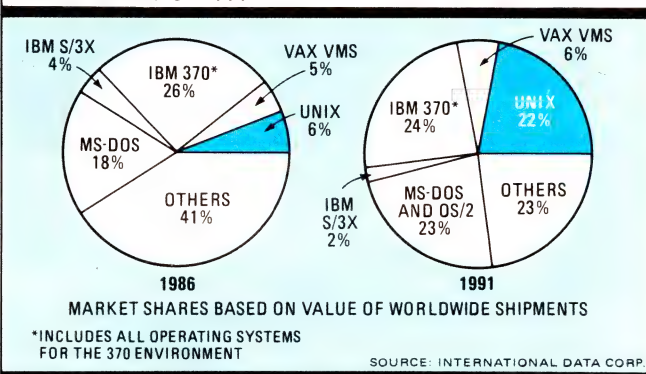
by Jeremy Young and Tom Manuel

likely emergence of a single Unix version for the Intel 80386 processor. This Unix is expected to give the OS/2 operating system being developed by IBM Corp. and Microsoft Corp. for IBM's PS/2 personal computers a run for its market.

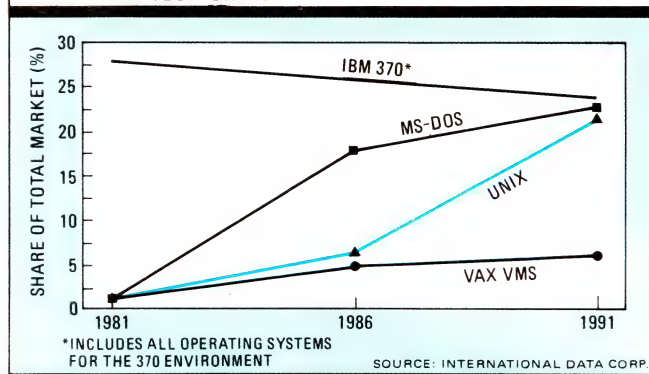
Unix is having a twofold impact on the computer industry: it plays a leading role as a standard operating system for software portability and it acts as a catalyst for the push for open-systems standards worldwide. Unix is a rallying point around which other standards, such as network file systems, windowing user interfaces, and networking computing are being created.

Emerging standards such as the X Windows networked windowing system, Sun's Network File System, AT&T's remote file system, the X/Open standards, and the IEEE's 1003.1 Posix standard, and many of the Open Systems Interconnection communications standards as well, are outgrowths of the striving for open systems that began with Unix. These standards at least

UNIX IS TAKING OFF . . .



. . . AFTER A SLOW START



work with Unix, if they are not actually parts of the evolving Unix operating system environment itself (see chart, next page).

Thanks in large part to the improvement in standards, the market for Unix hardware is doubling every year. International Data Corp. puts the total world's Unix market at \$6.2 billion last year. The Framingham, Mass., market-research company predicts that the worldwide Unix market will grow at a compound annual rate of 32% between now and 1991 to reach a total value of \$33 billion.

Until two years ago, systems sold with Unix as the primary operating system represented only about 2% of the total system sales worldwide. By the end of 1986, though, that figure was at 6%, says IDC. Now Unix is gaining smartly on other operating systems and will garner a 22% share by 1991 (see chart, previous page).

A surge of buyer willingness to jump ship

tions working on the problem as well. X/Open is trying to bring together a standard for Europe. An organization called /usr/group/, Santa Clara, Calif., is involved in similar efforts. Part of its effort was transferred to the IEEE to become the 1003 Committee, but /usr/group/ continues to work on other extensions to Unix, such as real-time and security features. The IEEE 1003 Committee expects to mail a draft standard called 1003.1 Posix for voting in November. The draft is already getting a lot of industry support.

As it stands now, however, Posix is not a full operating-system standard. It is a programming interface that defines a specific set of system calls—ways in which an application program can obtain specific services from the hardware—and a library of system subroutines. But Posix is new and incomplete. If the draft is approved, which seems likely, there will be a Posix standard that ensures some degree of compatibility among systems complying with it, but nothing like 100% compatibility. What it does, at this point, is make the job of porting an application from one machine to another easier, but far from automatic.

Version 1003.1 of Posix "is a minimal set of things under which you can write a fairly large number of applications," says Michael Tilson, president of HCR Corp., Toronto, Ont., a vendor of Unix software. The Posix committee is actively working on extending Posix. Internationalization, or incorporating the ability to accommodate a range of languages in Unix applications, "is everybody's bugaboo right now," he says. X/Open is leading these efforts on European languages, but it has come into conflict with AT&T and the ANSI committee that defines the C language used in Unix systems, Tilson says.

"The one danger of Posix is that people believe there's more to it than there really is," he says. "Posix is only a small subset of what Unix really is." For example, Posix omits network-interfacing, semaphore, and shared-memory features, all features specified in SVID.

But many are leery of depending on AT&T to define Unix, because AT&T could change it arbitrarily to suit its own computer architectures or simply to make trouble for the competition. "What Posix does," says Tilson, "is pin down some parts of Unix as defined by SVID so that AT&T won't be able to change them." Posix, as a standard controlled by the IEEE, goes a long way toward generating confidence in Unix as a stable standard.

One of the most promising standards pushes that is going on now, however, is not centered in any formal industry committee, but is happening through a set of liaisons between Intel, AT&T, Microsoft, and Interactive Systems. This is a Unix due soon for systems based on Intel's 80386 32-bit microprocessor.

AT&T contracted with Intel Corp., Santa Clara, Calif., to adapt Unix to the 386, which AT&T is using in PCs. Intel in turn subcontracted the job

WHERE UNIX HAS ALREADY WON

Type of technical computing system	Operating system		
	% Unix	% VAX VMS*	% other
Technical work stations	83	4	13
Minisupercomputers	75	19	6
Parallel processors	50	0	50
Supercomputers	72	2	26
Total	84	4	12
*VMS or VMS-compatible SOURCE: INTERNATIONAL DATA CORP.			

from proprietary systems to join the open-systems world is propelling Unix onto a steep upward ramp. Along with MS-DOS, the operating system for IBM PCs, Unix will catch up with the long-dominant operating systems for IBM mainframes by 1992 and leave Digital Equipment Corp.'s VAX VMS behind.

But strong standards are crucial to the growth of the Unix market, and there is still a great profusion of only barely compatible Unix systems. Seventeen years ago, researchers at AT&T Bell Laboratories, Murray Hill, N.J., began to distribute source-code copies to fellow researchers at universities and other labs. AT&T, not a computer vendor at that time, exerted no control over versions of Unix that were modified by others, and did not attempt to bring the resulting chaos of multiple Unix versions under control until about four years ago.

During the last few years, the software world has been finding out how hard it is to put something like Unix back together once unraveled. Much work has gone into creating a single Unix standard. AT&T has defined and created System V, and that is the most complete standard today, embodied in the System V Interface Definition (SVID), a suite of software that must all run on a system before AT&T will certify it.

But there are a number of industry associa-

to Interactive Systems Corp. of Santa Monica, Calif., which produced a Unix port called 386/IX. It is System-V.3-compatible, and can run MS-DOS applications.

Now Interactive Systems has a signed contract with Microsoft Corp., Redmond, Wash., to produce what it calls a "merge"—that is, a version of Unix that will run programs written for Microsoft's Xenix (both the 286 and the 386 versions) plus programs written for 386/IX, plus MS-DOS programs. The likely result will be a single, standard, SVID-certified Unix for all 386-based computers, with binary-code compatibility. In other words, programs written for one 386-based system will run on other vendors' 386-based systems without a porting effort and without recompiling. If this happens, it will constitute a small miracle—for the Unix world, anyway—and a major coup for Intel, which has been promoting such unification.

Interactive Systems expects to have the merged version ready in the first quarter of 1988, in time to compete with OS/2, says Heinz Lycklama, senior vice president of technology at the company and a member of the Posix committee. Although the merged 386 Unix will be based on System V, "we have added some Berkeley features to it," Lycklama says. Other Unix ports are available for 386 machines, but vendors of 386-based systems are very likely to migrate to the merged version, says HCR's Tilson. That means the 386-system community should have a unified approach to Unix inside of about one year, he believes. As a result, "the 386 stands to be the highest-volume Unix platform of them all," he says.

Tilson contrasts the 386 Unix situation with that surrounding Motorola Inc.'s 68020 microprocessor. There are many versions of Unix for the 68020; no one has made an effort to pull them together to make a standard. "There's a lot of variety, and no binary compatibility," he says, "which is kind of silly, since they're all running on the same processor."

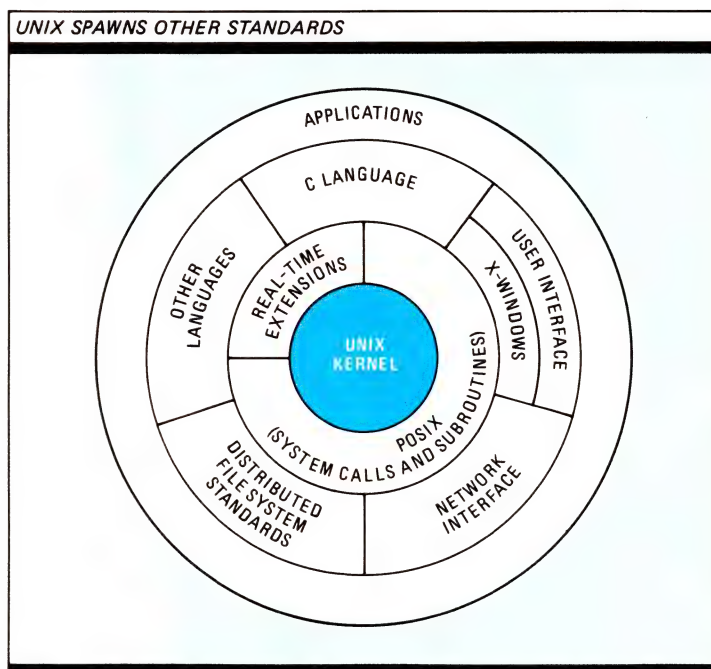
OS/2, the much-ballyhooed multitasking operating system for 386-based machines, may lose a big piece of market share to Unix. OS/2 is late, and the merged 386 Unix will be on the market as OS/2 arrives toward the middle of 1988.

There are already many applications that run under Unix, and applications for OS/2 may be some time coming. Both will run MS-DOS programs, but only Unix offers users the multiuser option. "You could have 10 MS-DOS applications running at once, as well as Unix applications. Something like that has the potential of short-circuiting OS/2," says Tom Greene, research-and-development manager at Apollo Computer Inc., Chelmsford, Mass. OS/2 suffered another blow recently when IBM itself announced plans to offer Unix for its 386-based PS/2 Model 80, to bring it in line with software standards for the technical work station market.

Some feel, however, that OS/2 and Unix could settle into different segments of the market. "Unix is the best solution for multiuser systems," says an executive at Milan-based Olivetti. "There's no competition between MS-DOS and OS/2 on the one hand and Unix on the other because MS-DOS, and probably OS/2, will be standard for single-user PCs and Unix for servers, minicomputer engines, and high-end work stations."

A standard for Unix that applies across many architectures, however, will take more time. "Unix has the potential of becoming a good standard," says Barbara Shelhoss, Apollo Computer's senior product manager for Unix. "The incompatibilities will eventually be worked out. The work the IEEE is doing on developing a vendor-independent standard is very important."

Ultimately, if the industry cannot present the user community with a standard Unix, the users



themselves will choose a standard. And a user-driven trend is emerging, a trend that can be seen in the actions of the Air Force. It recently issued a request for proposals for a huge contract: some 22,000 Unix-based departmental systems worth about \$3 billion.

The Air Force specified that the systems should be SVID-certified, with the provision that the vendor migrate to Posix compatibility when that standard matures sufficiently. Other major users, such as General Motors Corp., have set up similar requirements. All want a standard controlled by an industry body instead of one company, but they also see that Posix is not quite ready yet. □

Additional reporting by Paul Angiolillo, Lawrence Curran, John Gosch, and Jonah McLeod

UNIX:

A BIG EUROPEAN PUSH

Europe's computer industry is way out in front of the Americans in embracing Unix, thanks to its push for open systems; almost all major makers offer Unix-based systems

by John Gosch

Europe is wholeheartedly embracing Unix. Moving at a far faster pace than their American counterparts, European computer makers are pushing to establish the operating system that AT&T Bell Laboratories developed 17 years ago as the key component in their drive toward open-system computing.

Almost all the major European computer makers are fielding Unix-based systems, a fact reflected by the surging Unix market. The growth tends to be uneven, since some obstacles still remain to widespread use of Unix in mainframes, personal computers, and real-time systems, among others. Nevertheless, the growth of Unix seems sure to continue (see chart, below), because establishing it as a standard is in the best interests of virtually the entire data-processing community—users, hardware vendors, and software vendors.

Users like Unix as a standard because it promotes portability in software. That means they aren't tied to any particular vendor—they can buy the best hardware for their particular pur-

poses. Software vendors' interests converge neatly with those of users. They can write one version of an application and sell it to anyone with a Unix-based system, instead of adapting each application to a host of different proprietary operating systems.

For hardware vendors, a Unix standard promotes connectivity—it makes it much easier for them to link different machines. What is more important, though, is that promoting software portability and connectivity—in effect, establishing that all hardware is created equal—makes a Unix standard a potent weapon against dominance by IBM Corp.

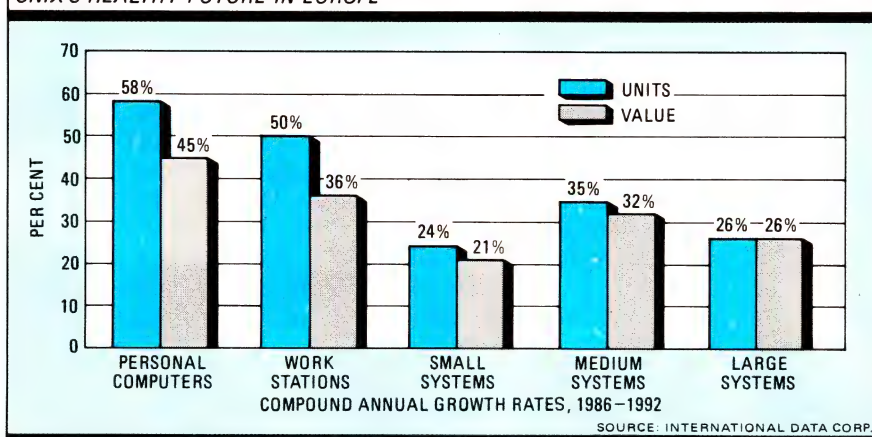
It was largely to combat IBM that European, and some American, hardware vendors originally established the X/Open Group [*Electronics*, July 10, 1986, p. 121], which has since become the X/Open Co. This organization has been working to establish a standard version of Unix, along with several related standards—notably one for a programming interface that is based on the IEEE standard, Posix.

X/Open's efforts have, of course, also served to promote more widespread use of Unix. Combined with the various other factors that are pushing Unix, the results have been phenomenal. "The Unix market virtually exploded last year," says Friedrich Dischinger, a market researcher in the Data Systems Division of Siemens AG in Munich. Analysts at market research firms such as Inteco in London and International Data Corp. in Paris put the number of Unix systems delivered in Western Europe in 1986 at around 50,000—an increase of some 120% over the previous year.

Support for Unix has been greatest in two areas: small- and medium-size multiuser systems with from 4 to 16 terminals, and single-user work stations for engineering applications, including computer-aided design, says Klaus Gewalt, executive director in the Data Systems Division of Siemens. In work stations alone, Unix shipments grew by 150%, according to Siemens's market researchers.

Virtually all the computer companies in Western Europe are committed to Unix. Siemens, for example, by mid-1987 had delivered more

UNIX'S HEALTHY FUTURE IN EUROPE



than 16,000 of its MX Series Sinix machines in Europe since the end of 1982, the year it began to offer Sinix, which is the West German company's version of Unix. That number makes the company Europe's leader in the Unix world.

Nixdorf Computer AG is also shaping up as a strong Unix contender. With its Unix-based Targon family of supermicros, superminis, and multicomputer and fault-tolerant systems, the West German company is demonstrating that Unix can be extended into bigger systems. Nixdorf has installed 250 of its Targon models during the past two years, which is just the beginning. "By the end of this year we expect to have 1,000 of them in place," says Hermann Johannes, product marketing manager for the Targon family.

Philips in the Netherlands is on the Unix scene, too. The company has installed about 500 of its Unix-based P9000 family of minicomputers, which are servers or departmental processors. "We expect to do around \$700 million worth of business with the P9000 per year by 1990," says Gerd Bindels, senior managing director of Philips's Telecommunications and Data Systems Division.

SOME OBSTACLES REMAIN

However, Unix has not gained ground everywhere. Relatively few mainframes run Unix because "mainframe operating systems offer much more than Unix can," says John Totman, Unix product manager for ICL plc in Bracknell, UK. In addition, Siemens's Gewald notes that "AT&T originally devised Unix with minicomputers in mind. It would require big investments to adapt it to large mainframes."

At the other end of the spectrum, Unix has not yet entered the established single-user personal-computer environment, largely because it was developed mainly for multiuser systems. In that market, the MS-DOS operating system predominates. Similarly, the multiuser orientation makes Unix unsuitable for real-time systems. For example, Force Computers GmbH in Otterbrunn, West Germany, which sells board-level computers primarily for real-time applications, supplies Unix only for software development for its target systems.

Other factors are also inhibiting Unix's growth. Gewald points out that when older operating systems do well on the market, companies are reluctant to push Unix. Also, defining a formal standard is in the hands of several different standards organizations, says Vesa Kousa, a product manager in the Information System Division of Finland's Nokia Group. "These organizations are working so slowly that development is passing them by," he says.

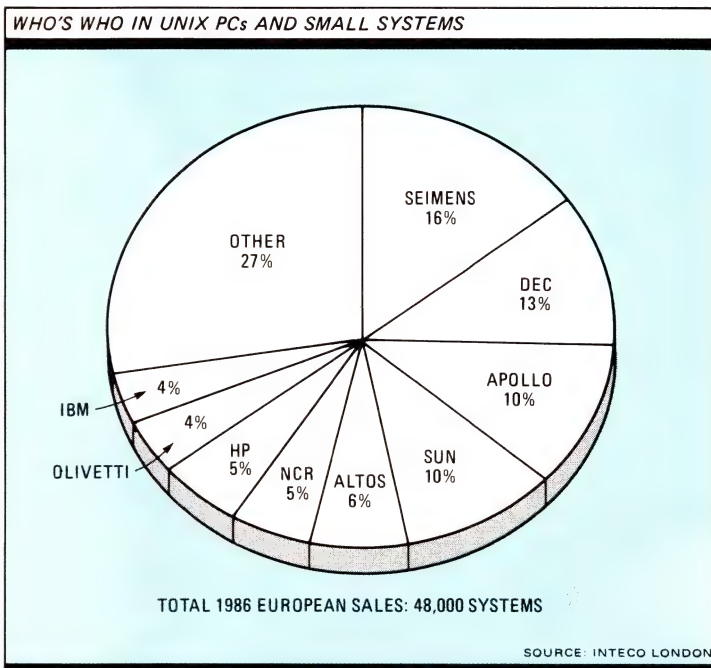
None of these obstacles is insurmountable. Unix is likely to spread further, faster. For one thing, "users are making it known that Unix would suit them best as a standard," says Totman at ICL. Gewald, at Siemens, agrees. The

reason is that Unix "gives them the freedom to switch to different suppliers and different hardware." It facilitates the portability of applications software, so users can employ programs written by a variety of software producers, including third-party software. These advantages, Gewald says, are the primary reasons for Unix's success so far.

For a software company, a standard like Unix reduces the cost of research, development, marketing, and support. And as Heinz Diehl, a technical manager at Nixdorf, points out: "It also provides such companies with greater access to new marketing channels and hardware markets."

For a hardware company, says Totman at ICL, a standard such as Unix is required to tie mid-range computers to personal work stations and mainframes. And such connectivity is vital: "In the future, markets will be dominated by the need for departmental computing, which will in turn demand applications portability at the source-code level as well as transparent networking among minis, from minis to personal terminals and desktops, and to mainframes—from MS-DOS through to top-range mainframes," he says.

"ICL sees the adoption of a standard operating-system interface as an integral part of the Open Systems Interconnection concept, where each node in a network should be able to support a standard application, irrespective of the architecture of the hardware in use," Totman says. "This would create a free and open market for applications and lead to a fully integrated market for hardware and software." He adds that Unix is not necessarily the best system technically to create this open environment—but it is available, it does the job, and its use is already widespread.



Promoting software portability and hardware connectivity means, in the words of Nixdorf's Diehl, that Unix "fosters internationalization of the industry." Eventually, the pressure for such internationalization will win out, says Siemens's Gewald: "In the long run, the demand for hardware-independent software will be stronger than the strategy of some computer makers to fence off their hardware base against the competition."

The computer maker most adept at defending

The drive in Europe for open systems is being led by X/Open, a consortium of 11 companies that account for a quarter of the global information-technology market

its hardware base is, of course, IBM. It is no secret that most of the major European computer companies feel that a Unix standard can help them break down those defenses. Using Unix to do so was one of the most important factors in the decision to found the X/Open Group, which was recently incorporated as X/Open Co. with headquarters in London.

X/Open was formed by 11 European and American computer makers—France's Bull, Sweden's Ericsson, ICL, Nixdorf, Italy's Olivetti, Philips, and Siemens, as well as AT&T, Digital Equipment, Hewlett-Packard, and Unisys, all of the U.S.—to define, promote, and enforce computer standards. It is now defining a Unix ver-

sion "that may well become a world standard," says Rob Morel, Philips's representative at X/Open's marketing committee.

The backers of X/Open represent a formidable force in the computer market. As executives at Olivetti point out, the combined revenues of the X/Open companies amount to a quarter of the worldwide information-technology market. And ICL's Totman says that the 11 founders of X/Open account for more than 40% of all midrange system deliveries in Europe.

X/Open, says an Olivetti executive at the company's headquarters in Ivrea, Italy, "is a pragmatic approach to standards for the Unix operating system, and it has defined in a very precise and detailed way a standard Unix environment." The group has adopted international standards that have already been agreed upon and has integrated them with specially adapted, commercially available interfaces, which are de facto standards. Also, X/Open is an institutional member of the IEEE 1003.1 Posix standards committee and has used that position to take a leading role in the definition of Posix, a standard programming interface for Unix.

The European Unix standard ratified by X/Open is based on AT&T's System V.2. The organization intends to work on the definition of a standard programming interface that will be completely compatible with the Posix standard and can be implemented on both AT&T System V and the Berkeley Unix systems.

Such a common transatlantic standard interface is vital, Totman says, and it looks as if Posix is emerging in that role. Initially, X/Open

defined a standard interface based on AT&T's System V Interface Definition, but Posix has the advantage of being in the public domain. It is not subject to the problems, real or perceived, that a proprietary system might have. Also, Posix is winning widespread acceptance among the major customers of the X/Open founders. Government agencies in the UK and Sweden are supporting it, for example, as are European Economic Community officials.

X/Open wants to include parts of Posix and other Unix systems into its version. Nixdorf's Diehl, who represents his company in X/Open, says this means that "as Posix elements come in, System V will fade away a bit." Eventually, what should emerge is a truly European version of Unix as the standard European operating system. □

Additional reporting by Peter Fletcher in the UK

UNIX IN JAPAN: LATE START, BUT PICKING UP

Unix is a late starter in Japan, but it already dominates the engineering workstation market. It is the operating system of choice on both domestic and imported systems. Although its use on other hardware is limited so far, activity is starting to pick up.

For example, Sony Corp. is entering the professional data processing market with eight Unix work stations. NEC Corp. has introduced a Unix-based operating system for one of its new 32-bit personal computers. Fujitsu Ltd. has a 32-bit computer that will support the combined Xenix/System V when it is available.

And if AT&T Co. has its way, Unix will start spreading fast. AT&T Unix Pacific Co., in Tokyo, has been promoting Unix in Asia now for three years, and its efforts are starting to pay off. The company's goal for this year was 30% growth, and it met that by August, says its president, Larry L. Crume.

AT&T Unix Pacific has been delivering the English-language version of its

386 System V since August. Recently, it announced that its Japanese Application Environment, JAE 2.0 for the 386, which allows the operating system to be used in any language, was to be shipped to three major accounts starting on September 15.

Another important push could come from the Japanese government, which is sponsoring a project called Sigma, with more ambitious goals than those of Europe's X/Open Co. Ltd. Sigma's members number some 175 companies, and include end users. X/Open, by comparison, has 11 members, all vendors.

Sigma so far has only developed version zero of a Unix V-derived operating system. But the sponsors are optimistic that in five years Sigma will produce a large user population of software developers. Sigma is expected to bring about a significant increase in Japanese software development productivity by providing a common development environment.

—Charles L. Cohen

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CHIPS & TECHNOLOGIES PLUGS INTO IBM'S MICRO CHANNEL

When IBM announced its PS/2 series of personal computers earlier this year, PC-clone makers as well as their chip suppliers were quick to say they didn't expect to encounter any significant problems in coming up with their own versions of the PS families or the chips that made that possible. But they made that claim before they took a good look at the Micro Channel, IBM's new expansion bus for PS/2 models 50, 60, and 80. On the face of it, Micro Channel seems to be totally incompatible with the IBM PC and PC/AT buses.

That didn't daunt Chips & Technologies Inc., the young upstart supplier of about 80% of the chips that have allowed clone manufacturers to take away big shares of the PC markets from IBM Corp. Now the San Jose, Calif., company is going to try to repeat history with the PS/2. This month, Chips & Technologies (see p.77) will introduce the first in a family of Micro Channel adapter circuits that it calls the MicroChips family.

To begin with, Chips & Technologies will offer these first three chips to equipment makers supplying adapter and accelerator boards and cards. But early next year, the company will use these chips along with additional members of the MicroChips family to build versions of the PS/2 models 50, 60, and 80 motherboards that it will sell to clone makers.

The MicroChips family initially will include generic and function-specific chips that will interface with the PS/2's asynchronous bus. With these chips, adapter- and accelerator-board manufacturers will be able to supply products that add features and capabilities not incorporated in the IBM computers, ranging all the way from additional memory and input/output channels to accelerator boards that boost performance. Each of these requires a different level of Micro Channel support.

Initially there will be three standard versions of MicroChips: the 82C611 (see fig. 1), the 82C612, and the 82C613, all fabricated in 1.5- μ m double-metal CMOS. The 82C611 is aimed at the memory, I/O, and multi-function adapter-card markets, says Raj Jaswa, senior product marketing engineer at Chips & Technologies. It is designed to support up to four I/O relocations and one memory relocation. Aimed at use on peripheral-con-

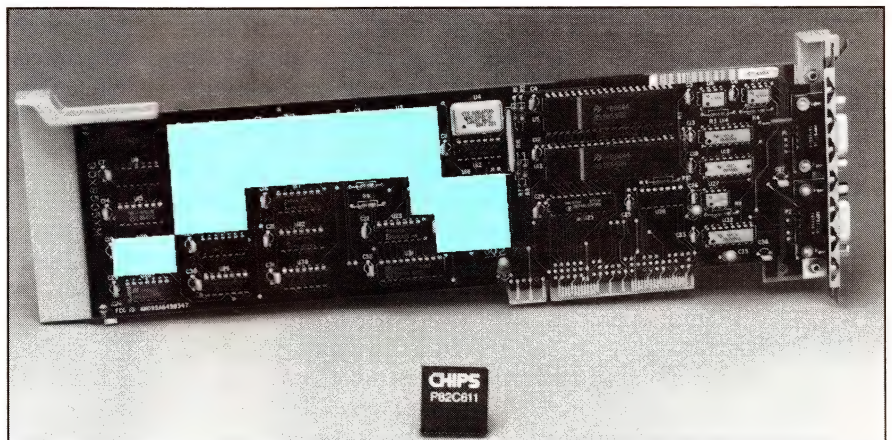
The PC-clone chip maker's three interface chips will enable adapter-card makers to add features to IBM's PS/2; an expanded chip set will make PS/2 clones possible

by Bernard C. Cole

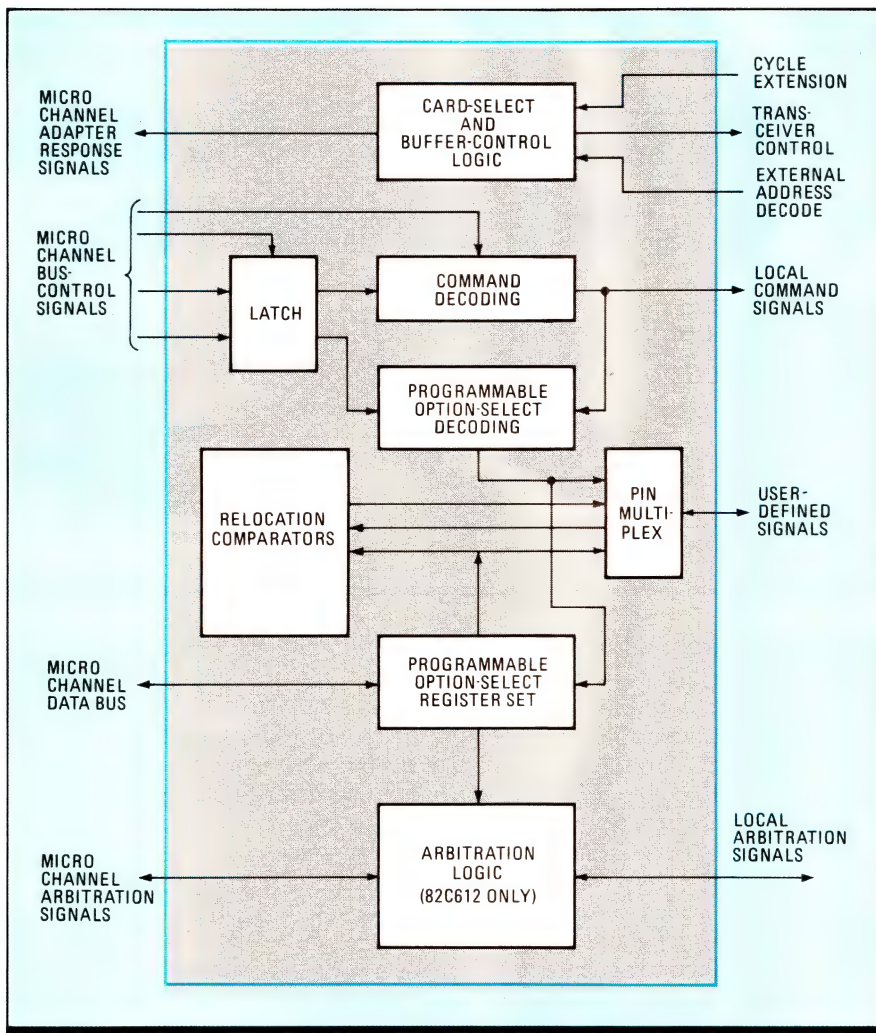
trol adapter cards for the PS/2, the 82C612 can support two I/O relocations and one memory relocation. Both parts will be available in sample quantities in late October and in production quantities in November. Available in the first quarter of 1988, the 82C613 is aimed at coprocessor and high-performance adapters. It will support up to two I/O relocations and one memory relocation.

Along with the standard versions, there will be application-specific MicroChips customized for very high-volume applications. For example, scheduled for introduction later in the year is the 82C574, a custom MicroChip that complements Chips & Technologies' new 82C570 single-chip implementation of IBM's 3270 terminal protocol.

On the face of it, the Micro Channel architecture represents a radical departure from the basic PC and PC/AT. The most significant departure is the fact that bus transfers on the Micro Channel are asynchronous, versus the synchronous scheme used in the PC, XT, and AT designs. "For us, this is less of a problem than most other chip manufacturers targeting the PC market, since very early in



1. SPACE SAVER. Chips & Technologies' 82C611, designed to interface with the Micro Channel in the new IBM Personal System/2, replaces 10 separate chips on this adapter card.



2. SOFT SELECTION. Every MicroChip includes programmable-option-select registers that allow software selection of particular features.

sions of the MicroChips include Micro Channel-compatible control-signal conversion and generation, software-controlled feature selection, and adapter identification support, plus a number of general-purpose registers for channel checking, synchronous ready-signal generation, memory relocation, and bus arbitration. The MicroChips will also incorporate multi-function pins to extend their utility to more diverse adapter environments than IBM is considering, says Jaswa.

The first Micro Channel feature that Chips & Technologies had to wrestle with was its use of coded cycle commands on an asynchronous bus instead of the more familiar memory and I/O signals used on the synchronous architecture of the AT, Jaswa says. Most available 80286/386 peripherals use decoded signals, so the MicroChips' logic decodes the bus-status signals to provide the more familiar commands.

To replace the DIP switches and jumper cables used for feature selection in the PC architecture, the PS/2 Micro Channel includes the POS (programmable-option-select) feature, implemented by means of an 8-byte register set for each card slot. Each

the game we shifted away from the synchronous approach to an asynchronous architecture," says Rob Catlin, system logic design manager.

While the Micro Channel has changed the way the hardware generates interrupts, the software interface remains virtually unchanged, Catlin says. In fact, rather than representing any radical breakthrough, says Jaswa, the Micro Channel bus is more a redesign of the PC/AT I/O channel that corrects past mistakes and adds new capabilities.

To address the needs of the variety of manufacturers of adapter cards for the synchronous PC/AT who now want to support the PS/2's asynchronous architecture, Chips & Technologies is segmenting the Micro Channel interface somewhat differently than IBM does. In the PS/2, says Catlin, the Micro Channel interface cards mix the generic handshaking signals and bus protocols with the circuitry needed to implement a specific function. "In our approach, we have partitioned the interface so that the Micro Channel signals and protocols common to all functions are contained on one generic chip," he says. And Chips & Technologies integrates those Micro Channel protocols specific to a particular function onto a chip that contains the logic for that function. All the various ver-

adapter card designed for the Micro Channel must contain at least some of these registers. The system board can select each card slot independently by driving a slot-specific signal. The same I/O addresses are used for each slot on the board.

The other POS registers defined as part of the Micro Channel fall into two categories: free-form registers to which IBM hasn't assigned specific functions and registers whose functions are dependent on the application to be implemented. On the MicroChips, some of the free-form registers are defined in order to cover various still-to-be-determined optional modes that the user may or may not want to employ, says Jaswa. These defined but unassigned register fields are grouped into MicroChips' internal registers: that setup gives the user the option of implementing these portions of the Micro Channel protocol in external POS registers on the adapter board.

On the PS/2, the system board reads and writes POS registers using a script language driven by an adapter description file (ADF). There is a different ADF for each type of adapter card. The system board must be able to tell what card type is installed in each slot, and so the IBM Micro Channel uses POS registers to return a 16-bit adapter ID.

The MicroChips implement these POS registers so that they can be incorporated easily in most standard adapter designs, including memory, I/O, and multifunction adapters; and master and slave DMA adapters. Catlin says each of these adapter types has somewhat different requirements with regard to signals from the microprocessor bus and the degree of external logic needed to make them conform to IBM's POS scheme. No one MicroChip can meet the requirements of all these types, but Jaswa says designers will find support for each adapter among the various family members.

Also incorporated onto the MicroChips is the Micro Channel protocol for providing ready-signal

generation. And, says Jaswa, the MicroChips not only provide the ready signal in the asynchronous mode required by the PS/2 bus, they also can be conditioned to perform in the synchronous mode.

The Micro Channel interface is designed to support up to 15 arbitrating devices contending for channel usage, Catlin says. These devices may be either masters or slaves. A master arbiter is a DMA device that supplies its own address and control signals when it is granted the bus. Slave arbiters are devices that must be used in conjunction with the system board's DMA controllers. MicroChips support both types of arbiters. □

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COMPANIES

HOW TO WIN ON IBM's TURF

If you want to know how to race a rampaging elephant and win, a good guy to ask for some tips might be Gordon Campbell, president, chief executive officer, and cofounder of Chips & Technologies Inc. of San Jose, Calif.

From the start, Campbell positioned his three-year-old company against IBM, supplying the chips that have let the makers of Personal Computer clones steal that market away from the Armonk, N. Y., giant. Now he has his eye on the PS/2 market. Chips & Technologies is introducing a family of interface chips that takes on the Micro Channel challenge (see p. 75). And by the first of the year, it plans to introduce a full chip set aimed at the high end of the PS/2 line, the models 50, 60, and 80. The company already has introduced chip sets aimed at the low-end PS/2 model 30.

If anyone has any doubts about the ability of the small company to take on this challenge, Campbell just tells them to look at the record. "We were started on only about \$3 million," he says. "Yet, by June of 1986, although we had only been shipping product for the last six months of our first fiscal year, we not only turned profitable, but had sales of \$12 million for the year." As of June of this year, the company racked up \$80.2 million in sales and averaged about 17% profit after taxes. And even with a number of competitors getting into the market—Faraday Electronics, LSI Logic,

VLSI Technology, Zymos—Campbell is confident that his company will remain dominant.

Campbell's formula for success is simple. First, don't play the other guy's game. Do what you do best, not what he does best. Second, anticipate the competition. Don't wait for IBM's shoe to drop, but anticipate where it will. Third, spend your resources wisely. Fourth, be fast on your feet.

As far as rule No. 1 is concerned, says Campbell, IBM's game is to keep things as static and unchanging as possible, with a family of products that meet a spectrum of needs. Another strategy it has, he says, is the use of vertical integration to reduce manufacturing costs and increase profit margins. "We obviously can't compete on the same terms," says Campbell. "Instead, we have developed a dynamic,



CAMPBELL. His first rule for playing against IBM: do what you do best, not what it does best.

rather than a static, product strategy, a family of products that are upwardly compatible and one step ahead in terms of performance."

As for rule No. 2, says Campbell, it is simply not enough to watch what IBM is doing and then come into the market with a chip set or a system that does it better. While that results in short-term advantages, you are always dependent on what IBM is doing, he says. "What you want to do is look at the long-term trends and anticipate IBM's future direction," he says.

Chips & Technologies' ability to stay one step ahead, technically, is a direct result of rules No. 3 and No. 4. Spending its money wisely, the company has not invested in its own fabrication facilities during its startup years. Instead, the company has invested in research and development and in tools to facilitate quick turnaround of designs.

Key to responding quickly to market changes is enough computing power to turn around designs quickly, says Campbell. For that reason, virtually every cent of the initial investment made in the company was poured into the purchase of two mainframes, an Amdahl 470 and an IBM 3090, giving the company an impressive 30 or 40 mainframe MIPS and 30 to 40 gigabytes of storage. Even something as straightforward as mask checking, which requires as much as 42 hours on a VAX-11/70, takes less than an hour on either the Amdahl or the IBM mainframes.

—B. C. C.



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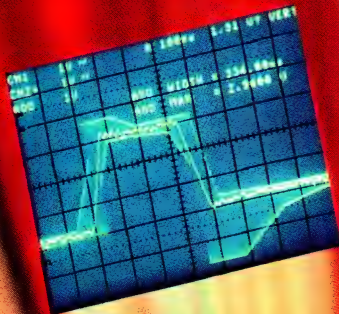
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Save on Delta; and see waveform changes virtually as *they happen* thanks to the 2430A's high update rate.

New Local Test features mean fast, accurate, automatic answers. Auto Setup takes the trial and error out of scope setup. Just one button sets up the 2430A to acquire and automatically display unknown input signals as you probe multiple points on a circuit. Auto Setup also simplifies your preparations for specific measurements.

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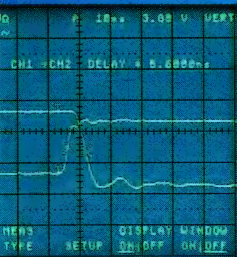
And you can take advantage of standard GPIO and off-the-shelf software to fully automate measurements and extend waveform analysis.

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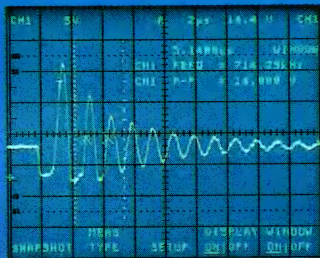
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Waveform Parameter Extraction allows you to make specific measurements on the windowed portion of a waveform. Here, frequency and peak-to-peak voltage measurements are made on two cycles of a damped sinewave. The cursors set the limits of the window.

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TECHNOLOGY OUTLOOK

THE DRIVING FORCE: THE INSATIABLE DEMAND FOR INFORMATION

On almost every technology front, the driving force behind new developments is the ever-rising demand for information. Huge amounts of data and information, larger than anyone ever dreamed of a generation ago, have to move faster and faster through processors and networks, then end up having to be stored. To accomplish this titanic task, semiconductor technology is moving ever faster toward speedier, more powerful processors and denser, more complex logic chips to manipulate this information. Memories must keep expanding in capacity to store this information, as well as to reduce the time that it takes to access it. Architectures are getting restructured to speed the execution of instructions to process it. And networks are quickly expanding and getting smarter so users everywhere can share this information.

The engineers and designers behind this revolution need information, too—and they are profiting from the advances in information technology. They sit at powerful work stations with high-resolution graphics, quickly designing and laying out complex chips and multilayer printed-circuit boards. They can mix or match vast libraries of proven functional block designs. Sophisticated computer-aided-design tools offer advice and guidance, so users can simulate designs in real time before they're implemented, then move them into production faster because prototypes usually work the first time. High-performance instruments acquire and manipulate test data, while monitoring production for any signs of trouble. Meanwhile, at the factory, information links the production line, the front office, and the customer.

For now, it's hard to see any slowdown coming in the demand for more information; it's also hard to foresee a slowdown in the rate of technology change.

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COMPUTERS

PERFORMANCE IS THE NAME OF THE GAME

Performance seems to be accelerating in computers. More and more, spec sheets are spelling out product power that runs in the millions of instructions per second—even at the desktop and work-station levels. Next year, architectural innovation will contribute as much or more to performance improvement as will radically changing semiconductor technology.

From this flurry of development activity a three-tiered hierarchy of interconnected machines is beginning to emerge. A multitude of powerful work stations dominate a low end that's widening, a bunch of machines in the middle concentrate on such services as computing, coordinating, filing, plotting, and printing, while at the top are the big guys: mainframes, supercomputers, and very fast specialized processors. Coming next year along with the performance kickers are more strides along the long path to smoothing the interoperation among multivendor systems. Interconnection, resource sharing, and interaction will still not be easy on many

Coming Soon

- Personal computers running at 10 mips and with 10 Mbytes of memory and 3-d graphics
- Work stations zipping along at 100 mips and sporting several 100 Mbytes of memory
- Single-user supercomputers delivering 100 or more megaflops to the desktop
- Direct-writing erasable magneto-optic disk drives with 1 Gbyte on 5.25-in. platters

networks, but a lot of work is continuing on methods to provide easier access to the wealth of functions offered by such networks.

The performance of personal computers and work stations will move up a notch next year thanks to the latest 32-bit microprocessors, bigger and faster memory chips, and advances in mass storage. Faster versions of the most popular microprocessors for personal computers—the Intel 80286 and 80386 and the Motorola 68020—coupled with the arrival of the Motorola 68030 and more use of cache memories and fast static random-access memories will allow personal computers to move into the multiple mips range (2 to 5 million instructions/s) late this year and early next. Shortly, personal computers

will move up to 10 mips as even more powerful microprocessors and faster memories come along.

Work stations, now in the 2-to-5-mips range with a couple hitting 10 mips, will break into tens-of-mips performance levels. To accomplish these hikes, designers will make use of architectural advances now embodied in high-performance chips and chip sets, such as reduced-instruction-set-computer techniques and the pipelining and memory-management schemes invented for mainframes. Today's examples include the RISC chips from MIPS Computer Systems and Sun Microsystems, National Semiconductor's 32532, Advanced Micro Devices' 29000, and Intergraph's Clipper. All of these chips boast on-chip caches, separate paths for data and addresses, memory management, and some degree of pipelining and RISC features. Also in this category is Inmos's T800 Transputer, which combines RISC architecture with on-chip memory, four communication links for multiprocessor designs, and a high-performance floating-point unit.

Of course, for work-station customers, there's more to performance than just mips. Bruce Imsand, vice president for systems development at Intergraph Corp., Huntsville, Ala., agrees that 5 to 10 mips will be readily available in work stations in 1988, but says other elements are just as crucial: "Features, displays, software tools, and efficiency in running a customer's application will be more important [than mips]. We've been mipped to death," he says.

Still, more mips mean more capabilities, so it's clear that higher speeds are an aim of makers of machines



COMPUTERS EVERYWHERE. Computers and work stations such as these from Compaq will be appearing in nearly all work places.

at all levels of the three-tier hierarchy. For example, in a couple of years there will be 100-mips work stations with several hundred megabytes of main memory and a gigabyte or two of mass storage. In mid-range computers, servers will be capable of billions of instructions per second and will be managing terabyte information banks. And within two years, supercomputers and special processors will be executing several billions of floating-point instructions/s. "Discussions of processor speed will shift from megaflops and mips," says W. Daniel Hillis, founder of Thinking Machines Corp., the Cambridge, Mass., startup that has already built its second version of the 65,536-processor Connection Machine. "Gigaflops will no longer sound exotic. People will discuss performance casually in 'bips' rather than mips in high-performance scientific computing."

As soon as early 1988, a whole new category—as yet unnamed—of super-powerful machines will be available. Whether they are called personal supercomputers, desktop supercomputers, or something else, they will offer tremendous power in both scalar and vector processing at the beck and call of a single user.

100 MIPS ON THE DESK

"This is truly an exciting time to be in the computer business," says J. William Poduska, founder and chairman at Stellar Computer Inc., Newton, Mass. Stellar and Dana Computer Inc., Sunnyvale, Calif., each are working on projects for "putting 20 to 30 mips on your desk—and that would have been unimaginable a few years ago," Poduska says. "And the day after tomorrow, it will be 100 mips."

Stellar's first product, described as a graphics supercomputer, is expected to debut late this year or early next. It will employ a four-stream pipelined processing architecture and use the Unix System V version 3 operating system. "I'm excited about the convergence of technologies I see contributing to ever-higher performance in computers and engineering work stations," says Poduska, who also founded Apollo Computer and was a cofounder of Prime Computer Inc. He cites gate-array, memory-component, and graphics advances as making major contributions.

Poduska says Stellar has a proprietary scheme that employs a high degree of pipelining for parallel processing using a complex-instruction-set approach. But he's quick to point out that if RISC architectures offered a more attractive alternative, Stellar would seriously consider switching. While he feels RISC is appropriate for single-processor applications, "CISCs will begin to come back into focus as they become more economical for graphics and vector processing. I think RISC architectures may have reached their peak, but that's an opinion, not a moral judgment. It's no different than deciding between CMOS and emitter-coupled logic."

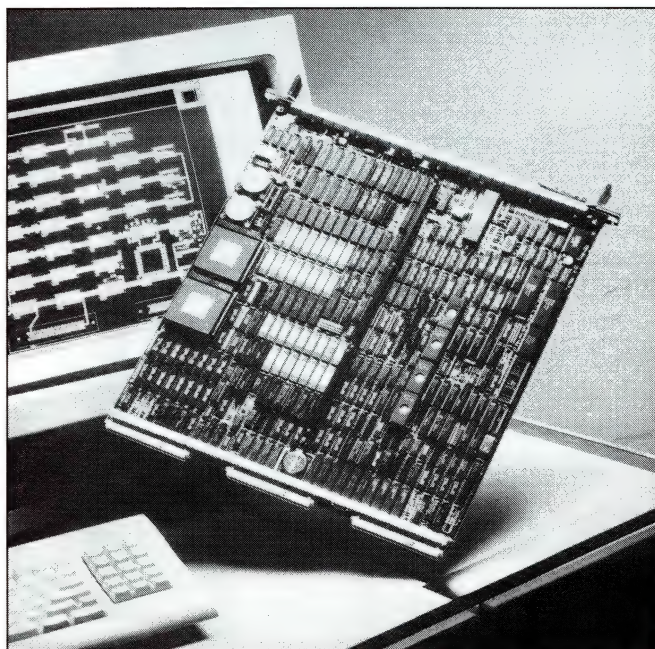
The RISC vs. CISC debate is too strident, anyway, says David L. Nelson, vice president and chief technical officer at Apollo Computer Inc., the Chelmsford, Mass., work-station and networked-computer-system maker. "I regard architectures and operating systems as tools—a means to achieving better system performance—and not as religions that demand slavish ad-

herence," he says. "There are good ideas in RISC, but it's not necessarily optimum when considered exclusively. RISC is a tool that we'll combine with others to achieve a high degree of parallelism and very high performance levels." Nelson notes that Apollo is working on a high-performance work station that promises "dramatic increases in performance levels by using combinations of hardware, including RISC but not exclusively RISC architecture." He says the machine may reach 40 mips.

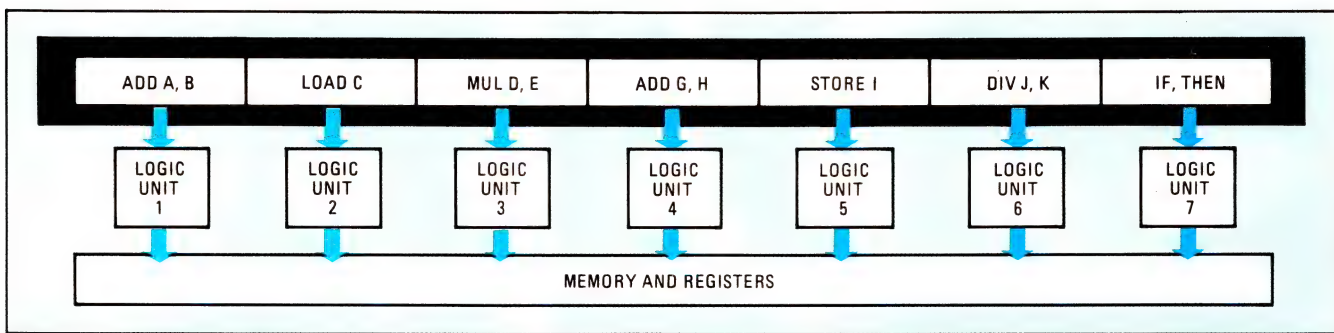
RISC and CISC may soon be competing for headline space with another emerging new architecture: the very-long-instruction-word machine. These computers have instruction words of several hundred to over 1,000 bits, compared with the conventional 32-bit or 64-bit instruction words. A few companies are delivering VLIW-based products, and the performance, achieved through completing many operations with each long instruction, is likely to spur development of others. Among the companies already in the field are Mentor Graphics Corp. and Trancept Systems Inc., which are using VLIW machines to build accelerators for network computing. Also, Floating Point Systems Inc. and Multiflow Computer Inc. both use VLIW architecture to build minisupercomputers. Multiflow's Trace computers perform 7 to 28 operations simultaneously.

Eventually, all computers except low-end personal computers will have to move into some form of parallel processing to continue to grow in performance. "It's the best way—the easiest way—to improve computing performance by an order of magnitude," says Carl Howe, manager of operating-system development at BBN Advanced Computers Inc., the Cambridge, Mass., manufacturer of microprocessor-based Butterfly parallel-processing systems.

Howe says a multiprocessor parallel-processing architecture allows systems to be easily and carefully configured for optimum processing power, and those



PERFECT 10. Work stations are moving to 10 mips and above. One of the first is this Sun 4 with its single-board, 10-mips RISC processor.



BIG WORDS. The Multiflow Trace with instruction words that process from 7 to 28 operations exemplify very-long-instruction-word architecture.

systems degrade far more gracefully than does a uni-processor system. "With a VAX, for example, if you have a failure in the cache memory, the system is down; with a Butterfly, the same kind of failure simply means you have one less processor to work with. In a 64-processor configuration, that means you've lost just 2% of your processing power."

Many parallel-processing architectures are being tried out, and there are several parallel machines on the market, including Thinking Machine's Connection Machine. However, the changeover of all computers to parallel processing will be gradual unless there is a

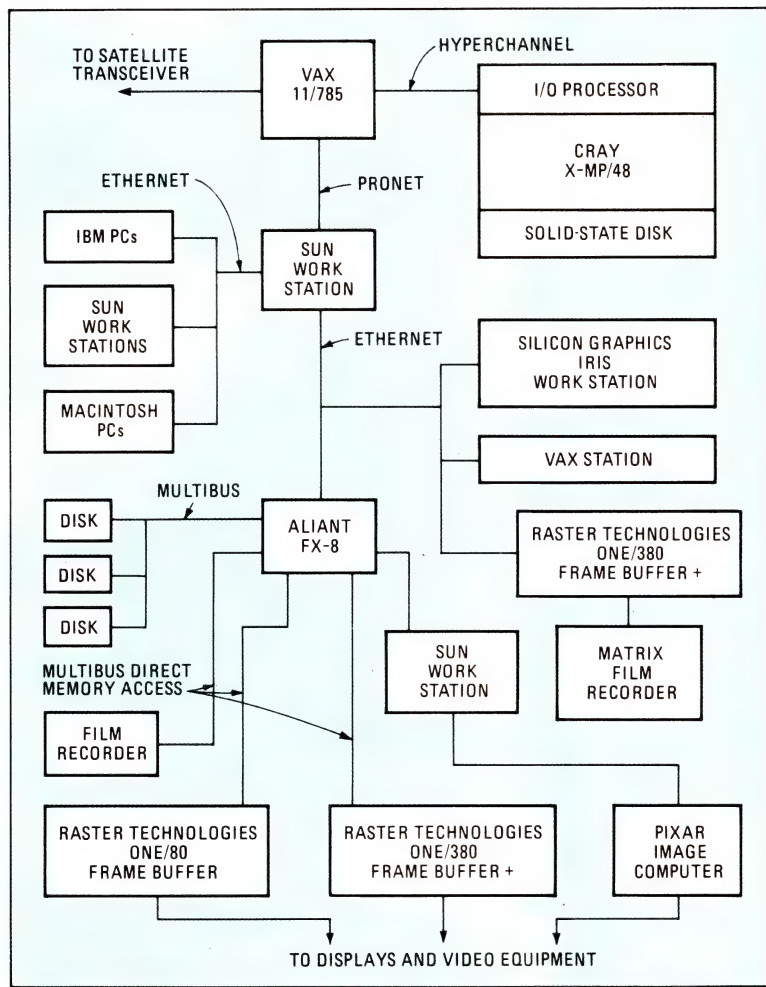
major breakthrough in converting and writing software to work in parallel.

Magnetic disk drives, long the mainstay for computer mass storage, will keep their dominant position for a number of years yet. Optical disk drives of the write-once variety will begin to play a bigger role in several market niches. Danny Hillis of Thinking Machines expects optical mass storage using the write-once read-many approach will be a significant technology in the next two years. "I think we'll see substantial amounts of parallel mass storage—tens of gigabytes—in that period," he says.

Another new storage technology, combining magnetics and laser optics, is about to emerge: erasable magneto-optic disk drives. A few 13-cm-diameter (5.25-in. form factor) magneto-optic disk drives have been announced and will start being delivered early next year. Typically they use both sides of a disk to store 650 Mbytes of data. But because two passes have to be made to first erase then to write new data, the average access time is 5 to 10 times slower than today's high-performance magnetic disk drives—100 ms versus 10 to 20 ms.

But there is a breakthrough in the wings for magneto-optic technology called direct overwriting, which will make these drives competitive with magnetic drives in access time. "Direct-overwrite magneto-optic drives with average access times matching Winchester [magnetic drives] speeds are about two years behind the initial magneto-optic drives, which have just been announced and will be available next year," says Mark H. Kryder, professor of electrical and computer engineering at Carnegie Mellon University in Pittsburgh, a leader in research on magneto-optic technology. "There is a lot of interest now in our work by industry—activity is underway in a number of companies," he says.

Another trend likely to accelerate is the transformation of computer systems into massive conglomerates of multivendor equipment and software. And these networks, rather than the operating system, will begin serving as the application interface in computing, says Craig Mundie, the vice president of marketing at Alliant Computer Systems



CONGLOMERATE. Hierarchical systems of many products such as this advanced visualization facility at the University of Illinois will be commonplace.

Corp., the Littleton, Mass., manufacturer of minisupercomputers for the server tier. "As a consequence, the instruction set of a processor will fade as an issue," says Thinking Machines' Hillis. "Today, the first thing people ask about a processor is [what is] the instruction set; it will become the last thing they ask."

One example of network computing is Apollo's Open Dialogue network-management and user-interface software, which allows user interfaces to be developed and adapted to personal-computer and workstation platforms from major vendors. "Work stations from those vendors now encompass the Unix, VMS, and MS/DOS operating systems," Apollo's Nelson says. "Open Dialogue allows a user to construct an application that runs across all of them at once and on only one of them at another time. So we're evolving a concept of an application that is a dynamic animal that can be spread across different machines and operating systems."

Alliant's Mundie points out that seamless integration is coming between personal computers and the server-level machines. For example, Sun and Apollo work stations and PCs now plug into an Ethernet, and the files of all of them can reside on an Alliant system that is driving a graphics output in a PC window. "We've never had that tight a coupling before," he says. Mundie says that a good prototype for the interconnected three-tiered system exists at the National Center for Supercomputer Applications at the University of Illinois at Champaign-Urbana. That installa-

tion, called the advanced-visualization facility, links various work stations at the lowest level with an Alliant FX/8 server system, several graphics and image coprocessors and film recorders in the middle, and a Cray X-MP/48 supercomputer at the top tier.

"An important area needing improvement is the way graphics data is visualized on the screen," says Stellar's Poduska. This is an area that his company is addressing, although he will not tip his hand as to how. "We need to render surfaces better on the screen so that engineers can see, for example, the edge of a turbine blade and how it might be flawed by high temperatures, so that they can build a better blade. It takes a lot of computing power, input/output capacity, and strong graphics capability to show the engineer what the data means—which is what computing is all about."

There will be two main developments in high-performance graphics in the coming year or two, predicts Louis Doctor, president of Raster Technologies Inc. in Westford, Mass. "The fastest systems will get faster, and cheap systems cheaper—but the fast ones won't necessarily get cheaper," he says. "For roughly the same amount of money, there will be dramatic improvements in high-performance 3-d graphics—by at least a power of 10 and probably more like 100 in horsepower. . . . Today's systems are nowhere near fast enough to interact with the complex models needed for today's simulations and analysis." —Tom Manuel
Additional reporting by Larry Curran and Paul Angiolillo

SOFTWARE

A BATTLE OVER OPERATING SYSTEMS

The world of software technology usually moves slowly, improving functionality here, reliability there, taking one small step at a time along the paths of long-term trends. But next year, at least one set of events is certain to stir up action in the software community. Two operating-system environments are set to arrive that cut loose the minicomputer power of the Intel 80386 microprocessor: OS/2 from Microsoft Corp. and IBM Corp., and a standard version of Unix. A battle for market share is likely to ensue, involving not only OS/2 and Unix, but also their associated windowing systems, the Presentation Manager and X-Windows.

On another front, recent trends in computer architecture toward both parallel and reduced-instruction-set computers depend heavily on developments in languages and compiler technology to make good their

Coming Soon

- OS/2, IBM's long-awaited operating system tailored to Intel's 80386 32-bit chip
- Compiler systems that bring many high-level languages to a new computer—quickly

high-performance promise. Advances in the ability of compilers to optimize the performance of application programs will be seen next year.

The 386 microprocessor from Intel Corp., Santa Clara, Calif., holds out big performance promises that are not yet being realized. Current 386-based personal computers are running applications written for the MS-DOS environment, essentially acting as fast 8086 processors. But MS-DOS only allows 640 Kbytes of address space for each program; the

386 is awaiting far more ambitious applications under OS/2 and Unix that can make use of its 4-gigabyte logical address space.

OS/2 is late and getting later. Originally slated for delivery at the beginning of 1988, it is now estimated to arrive toward the middle of the year. But Microsoft and IBM can't afford to hold up OS/2 for long, because a standard Unix System V for the 386 is due

during the first quarter (see p. 67). Unix may well swoop down from the minicomputer and work-station markets in which it is already strong and move in on OS/2 in many of the high-end personal-computer markets, boasting higher functionality—most notably, multiuser capability—and a body of existing software.

The success of 386 Unix depends to some degree on how quickly the X-Windows windowing standard can be solidified, adopted, and supported by user interfaces and application software. When OS/2 arrives, it will have Presentation Manager up and running as a de facto standard. Both windowing systems, along with a few competitors, aim at making possible in networked environments the ease of use that is the hallmark of Apple Computer Inc.'s versatile graphical Macintosh user interface.

Although X-Windows has rivals, most observers are betting on it to become the Unix standard, and a lot of work is going into shaping it up for that role. Many modifications have been suggested in recent months, and a new version is due by January.

Version 11 is a "fairly complete redesign," says Robert Scheifler, co-developer of the system at the Massachusetts Institute of Technology. It adds more graphics functionality and extensions to allow easier customization of the look and feel of the user interface that vendors build on top of it. "The next hurdles are tool kits and user interfaces," he says. "There's a lot of quality software [for X-Windows] coming down the pipe in the next three to six months." Researchers from Digital Equipment, Hewlett-Packard, and MIT are preparing Version 11 for review by the American National Standards Institute as a possible standard. They are also creating the X Toolkit, which will make it easier for software developers to work with X-Windows. And 11 companies are cooperating to define a 3-d graphics extension.

One big advantage of Unix and X-Windows over OS/2 and Presentation Manager is that Unix can run on bigger machines as well as on the 386 computers, resulting in a broader range of performance choices for the user. Many such machines, ranging from work

stations to supercomputers, are based on parallel and RISC architectures, and for them performance is of the essence. Behind that performance will be increasingly sophisticated compiler technology.

RISC architectures depend heavily on optimizing compilers because the machine instructions themselves do less than those of conventional computers: less is accomplished in a single machine-instruction cycle, though the cycles come faster. It takes more machine instructions to execute each high-level-language instruction; and as the number of executed instructions grows, it is more and more crucial that the compiler put them together efficiently.

Compiler technology is improving step by step, making it easier to bring a family of languages to a new computer more quickly, and bringing better and more reliable optimization techniques to bear. In 1988, researchers should come closer to developing a truly broad family of high-level-language front ends linked to a family of architecture-dependent code generators by an intermediate-code representation. Such multi-language compiler systems have been attempted before, but have not fulfilled their promise in terms of breadth and performance. But it appears that compiler specialists are poised to complete the daunting task of putting the pieces together to produce an extensive family of practical, reliable high-performance compilers.

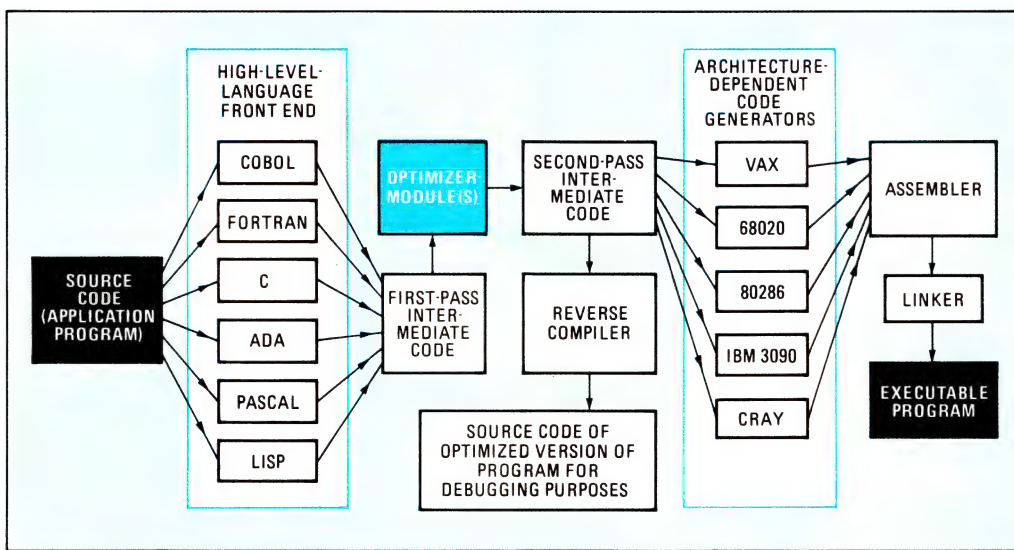
For one thing, optimization techniques are getting more sophisticated, producing faster executable code. More optimizers will take into account the dynamics of a program, for example. This means the optimizer considers concrete data about how often branch instructions are executed a certain way, or how many times particular loops are run in real-data situations, when it rewrites the program.

Debugging problems produced by optimization will be addressed as well, as automatic optimizing compilers come into wider use. One example is the reverse compiler, which produces a readable source-code version of the program after it has been rewritten by the optimizer. This makes it easier for a programmer to debug the

software. Without reverse compiling, it's hard to know what the optimized program is up to; it's likely to be different from the original program. Parallel computers particularly need advanced language-compiler technology, to get more software that takes advantage of their speed. New extensions of high-level languages are needed in standardized form, and adoption of such standards will be seen next year.

—Jeremy Young

Additional reporting by Paul Angiolillo



COMPILER FAMILIES. Multilanguage, multiarchitecture compiler systems are getting smarter, more practical.

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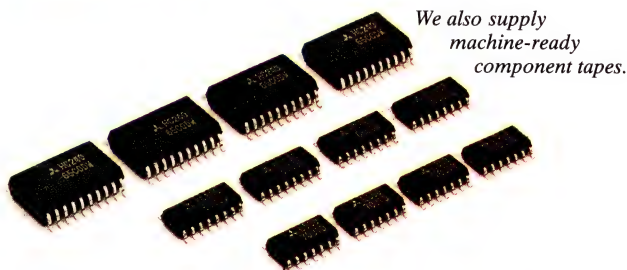


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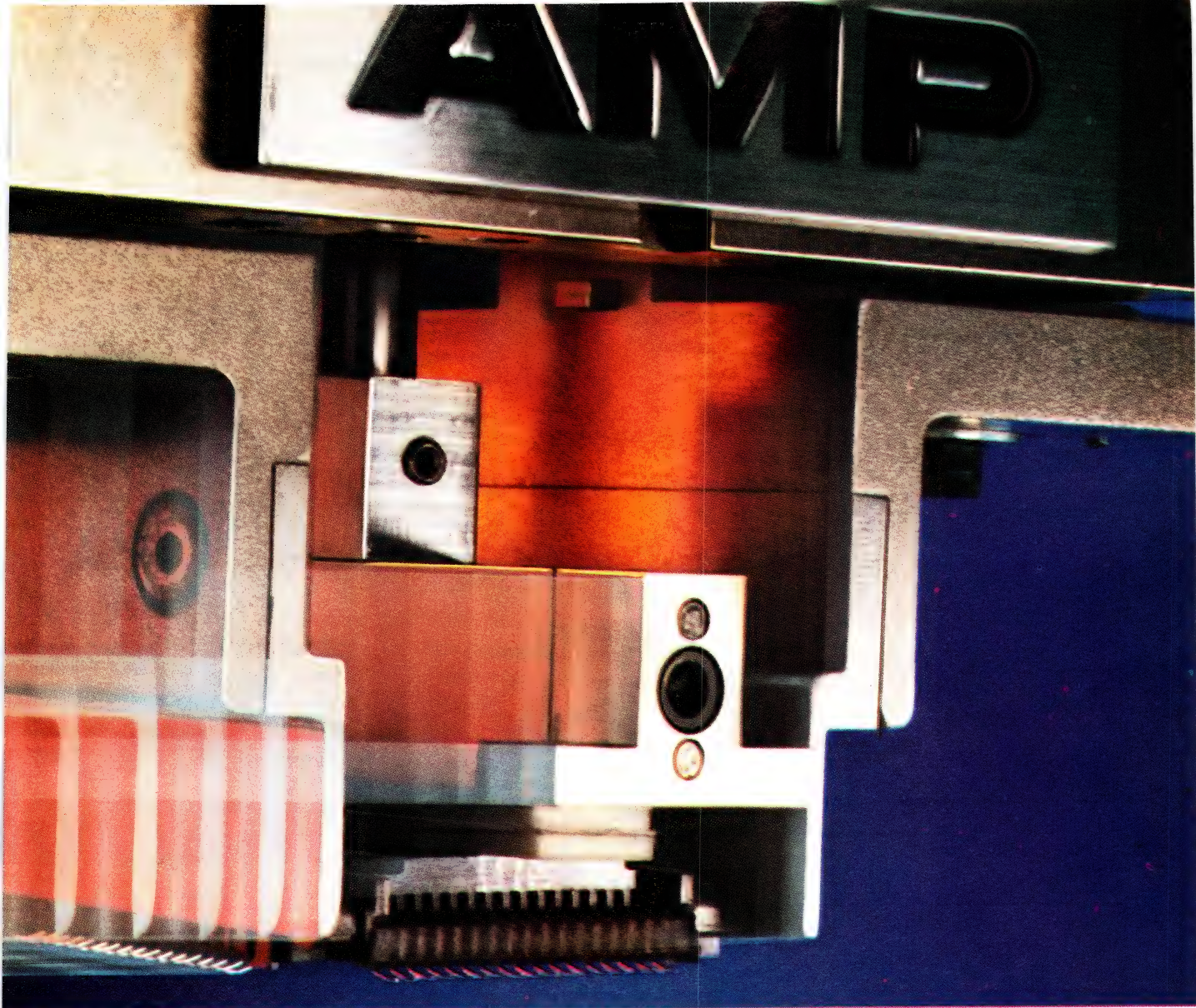
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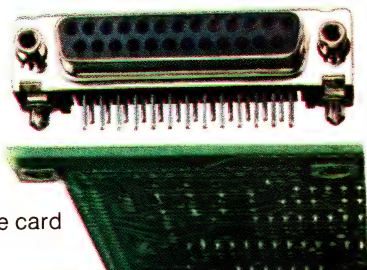
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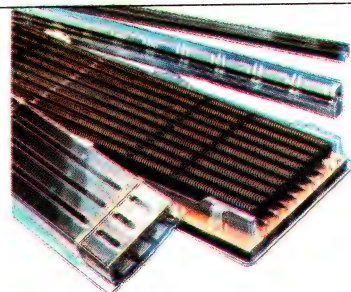
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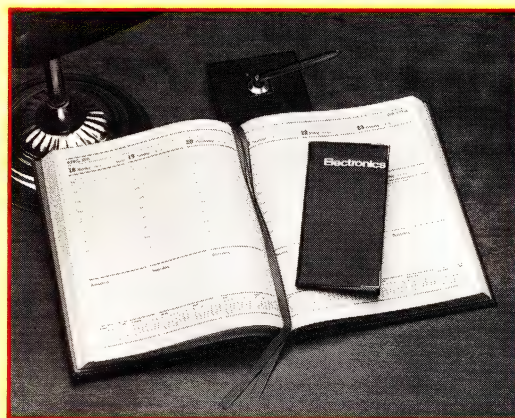
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SEMICONDUCTORS

THE WALLS COME TUMBLING DOWN

The coming year may go down as the point at which the semiconductor technology walls came tumbling down. In almost every area, the boundaries among separate disciplines, product types, processes, and design techniques are blurring, if not crumbling: between systems and components, between CMOS and bipolar, between static and dynamic random-access memory, between EPROMs and EEPROMs, between memory and logic, between custom and semicustom and standard products, and between traditional analog and digital circuitry.

Next year an increasing number of semiconductor firms will begin to introduce standard, semicustom and custom products based on next-generation CMOS processes with 0.8- to 1- μ m design rules, blurring the demarcation between exotic high-performance technology and standard commercial applications. Currently, only companies in the high-performance end of the CMOS business, such as Performance Semiconductor Corp. and Cypress Semiconductor Corp., are introducing memory and logic products based on such aggressive processes. But they will be joined in the submicron club by Intel, LSI Logic, Motorola, and Texas Instruments, as well as several Japanese companies. This burst of activity will result in semicustom parts with as many as 200,000 gates, compiler-based standard-cell-based designs approaching 450,000 gates, and full-custom and handcrafted stan-

Coming Soon

- Commercial CMOS ICs based on submicron design rules from a number of companies
- First samples of 4-Mbit dynamic RAMs, and the first experimental 16-Mbit designs
- Merging of logic and big memory blocks that will help boost system performance

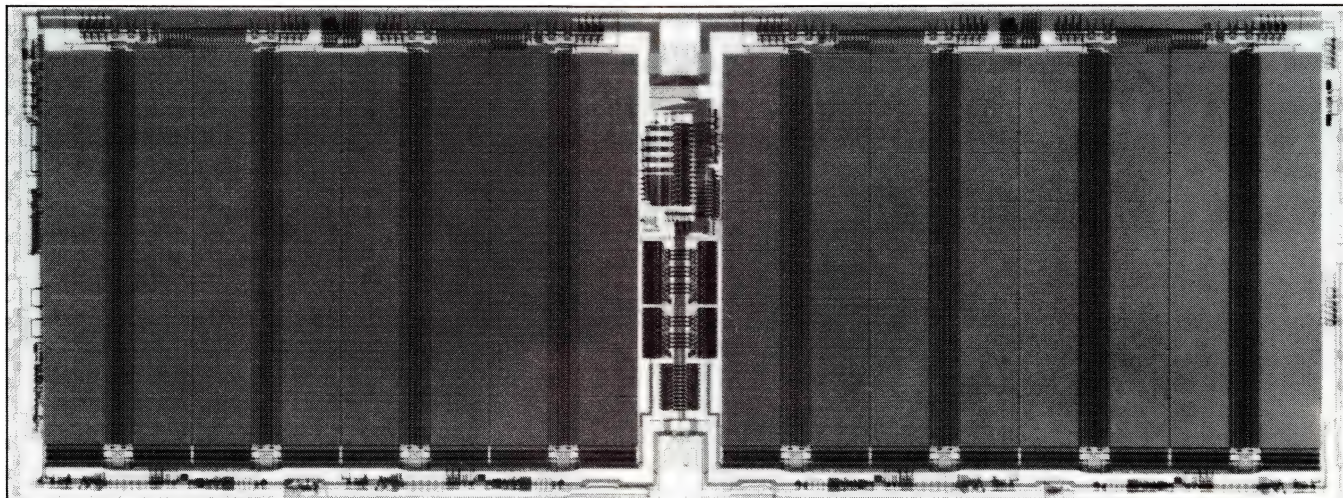
dard designs exceeding 500,000 gates, says James Meindl, vice president and provost at Rensselaer Polytechnic Institute in Troy, N. Y.

On the bipolar side, companies such as Advanced Micro Devices, Fairchild Semiconductor, Ferranti Interdesign, Honeywell, and TI are looking at sub-2 μ m device sizes. Their aim is to move late next year to a new generation of circuits, mostly based on gate arrays and standard cells, that will feature densities as high as 50,000 to 100,000 gates.

Among the most dramatic examples of the consequences of the move to smaller geometries will be

the continued advances in SRAM and DRAM densities. Even as 1-Mbit DRAMs from suppliers as diverse as Fujitsu, Hitachi, Motorola, NEC, Siemens, SGS, and TI replace 256-Kbit chips as the hot commodity part, these companies will be pushing to the sample stage with a first generation of 4-Mbit DRAMs. And following the early lead of Nippon Telegraph & Telephone Corp., at least two Japanese semiconductor companies will enter the ring in the coming year with experimental 16-Mbit designs.

To achieve these higher densities, at least a dozen or so new one-transistor cell structures have been proposed, says C. N. Reddy, president and founder of Alliance Semiconductor Corp., San Jose, Calif. All of them will require significant technology advancements in such areas as trench capacitor and transistor



FIRST GENERATION. Samples of 4-Mbit dynamic RAMs like this 70-ns chip from Fujitsu should appear in 1988.

technology, device isolation, and submicron lithography, he says. Although trench technology was proposed for 1-Mbit designs, engineers have found ways to get reliable circuits at reasonably high yields without the use of such esoteric procedures, says Reddy. At the 4- and 16-Mbit level, however, it will be another matter. There, trenches are likely to become mainstays, both as part of the basic cell and as an isolation technique.

HERE COMES THE FLASH EEPROM

During the coming year, ultraviolet-erasable and electrically erasable PROMs will continue to increase in density—mainly in CMOS, with n-MOS versions rapidly declining in popularity. As with SRAMs, the hot commodity part will be the 1-Mbit device. Also beginning to emerge in commercial form will be the first 2- and 4-Mbit versions. About one generation behind, but no less impressive, will be the emergence of floating-gate EEPROMs at the 512-Kbit level.

But the most startling developments will be in flash EEPROMs, and they will threaten the dominance of both traditional EPROMs and EEPROMs, says Richard Pashley, general manager of Intel Corp.'s EEPROM memory-business group in Folsom, Calif. Combining the hot-electron writability of EPROMs and the floating-gate erasability of the EEPROM, 256-Kbit flash EE-

PROMs are now available from only one supplier, Seeq Technology Inc. in San Jose. However, a 512-Kbit version is under development at Exel Semiconductor Corp. of San Jose, and Intel is said to be developing its own variation, which will allow the fabrication of flash EEPROMs at the 1-Mbit level and beyond.

The flash EEPROM offers less endurance: 100 to 1,000 write/erase cycles versus 10,000 to 100,000 or more for traditional floating-gate EEPROMs, says Gary Rauh, manager of strategic marketing at Seeq. But this part could raise the density of EEPROMs beyond the present 256-Kbit levels to the level of UV-based EPROMs. "If the present potential of equivalency with EPROM in yield and feature sizes proves out, the question is: who needs an EPROM?" he says. And for those who do not need the massive 100,000 cycles and the greater durability specifications of EEPROMs, "the question arises as to who needs traditional EEPROMs as well," says B. K. Marya, president of Catalyst Semiconductor Inc., Santa Clara, Calif.

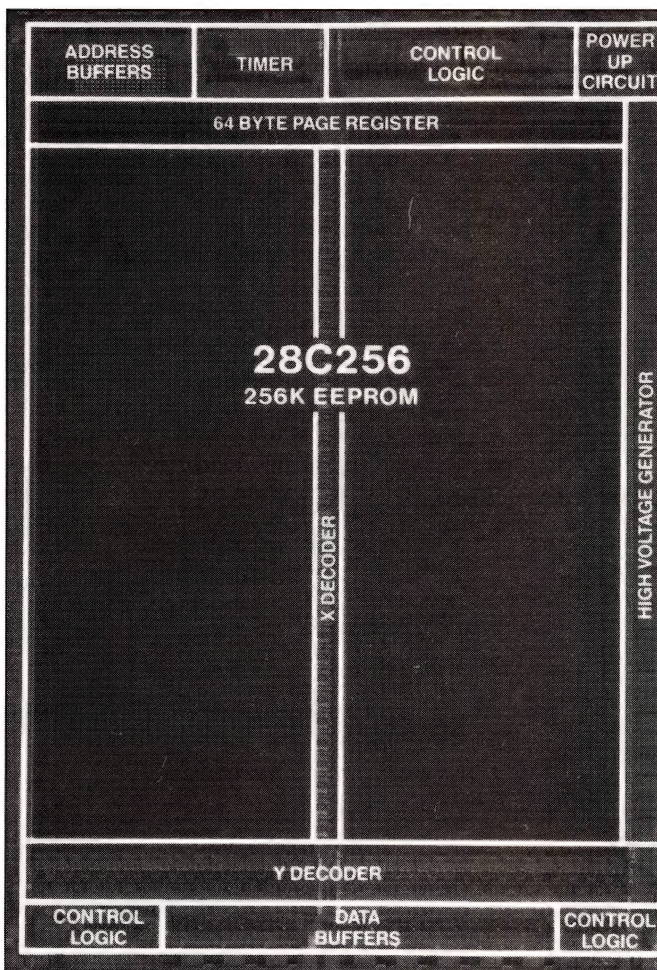
The availability of such high-density flash EEPROM technology will also significantly affect the design of microcontrollers, says Marya. "With the availability of such large amounts of nonvolatile but alterable memory, it will now be possible to build controllers with extremely large program and data memories, greatly expanding the range and sophistication of the functions they perform," he says.

Also affected will be programmable logic devices. Right now the only way to get 10,000-gate densities in PLDs is with SRAM-based designs, says Douglas Fairbairn, vice president and general manager of VLSI Technology Inc.'s ASIC Division in Milpitas, Calif. "With the emergence of the flash EEPROM, it now appears possible to build extremely high-density PLDs that are not only electrically erasable and nonvolatile, but comparable in density to gate arrays," he says.

The boundary between logic and memory circuitry will be getting fuzzier during the following year. On the memory side, more and more special-application SRAMs and DRAMs will be emerging, incorporating a great deal more intelligence. On the digital side, standard, semicustom, and custom designs are embedding larger and larger blocks of memory on chip.

The driving forces in both cases are the availability of higher levels of integration and the need for higher speed. On the memory side, as processor speeds increase, there is a greater need for higher-speed memory to reduce wait states. Interconnection delay time is the limiting factor, so it makes sense to incorporate the external logic onto the same chip as the memory. On the digital side, the same reasons apply to embedding the memory into the logic. And as the level of integration increases, customers demand more and more of the system, including memory, to be implemented on fewer and fewer chips.

As a result, 1988 may well be the year that smart memories begin to take off and accelerate the fracturing of the memory business into application-specific and system-specific niches, says Thomas Goodman, director of applications engineering at Vitelic Corp. of San Jose. Already there are such smart memory chips as dual-port SRAMs, cache-tag SRAMs, and SRAM-based



BIG FLASH. Seeq's 256Kbit flash EEPROM is the largest memory of this type currently available—but bigger ones are in the works.

first-in, first-out buffer memories. Now, says, Goodman, semiconductor makers will be turning out DRAM-based FIFOs, counting RAMs with onboard arithmetic logic units, and content-addressable memories. Indeed, he expects that the SRAM portion of the memory market will begin to fragment into large-volume commodity products on the one hand and more niche-oriented markets that can be addressed with CAD-based semicustom methodologies on the other.

On the logic side of the house, the coming year will see application-specific standard, semicustom, and custom circuits incorporating larger and larger amounts of memory, usually SRAM. This move will ameliorate some of the inherent speed limitations in present systems, such as package-to-package data-transfer problems, input/output level translation problems, and signal-communications and bus-timing problems between the standalone memory and the rest of the system.

GETTING SERIOUS ABOUT BICMOS

After years of fiddling around with mixed digital biMOS and biCMOS processes in the laboratories, more and more mainstream companies are getting serious about the merged-process technology. The popularity of biCMOS is increasing due to both short-term and long-term trends, says Andrew Wang, chief technical officer and cofounder of Saratoga Semiconductor Corp. in Cupertino, Calif. Over the short term, such companies as AMD, Fairchild, Fujitsu, Hitachi, Motorola, Signetics, and TI see it as a way to extend high-speed bipolar technologies such as emitter-coupled logic to higher densities at lower power. Over the long term, such companies as Cypress, Intel, and Signetics are looking to biCMOS as an alternative to pure CMOS at the 0.5- μ m level. While it is technically feasible to build viable CMOS transistors at the 0.5- μ m level with sufficient drive capability, it is getting incredibly expensive in terms of equipment cost, Wang says. BiCMOS is a way of getting sufficient drive capability at about the same geometries without as extensive an investment in equipment.

The most immediate impact of biCMOS will be in fast SRAMs, says Charles Hochsteder, product planning manager at Fairchild's Memory Products Division in Puyallup, Wash. "Currently bipolar TTL- and ECL-compatible SRAMs are stalled out at 64Kbits because of power dissipation and packaging problems," he says. "With biCMOS-based ECL memories, densities as high as 256Kbits to 1 Mbit are possible within the next year or two, with little or no sacrifice in speed."

As integration levels continue to climb, 1988 will see a continued blurring of the boundary between standard parts and custom and semicustom products and the emergence of the semistandard IC. The leader in implementing a semistandard approach to meet the custom require-

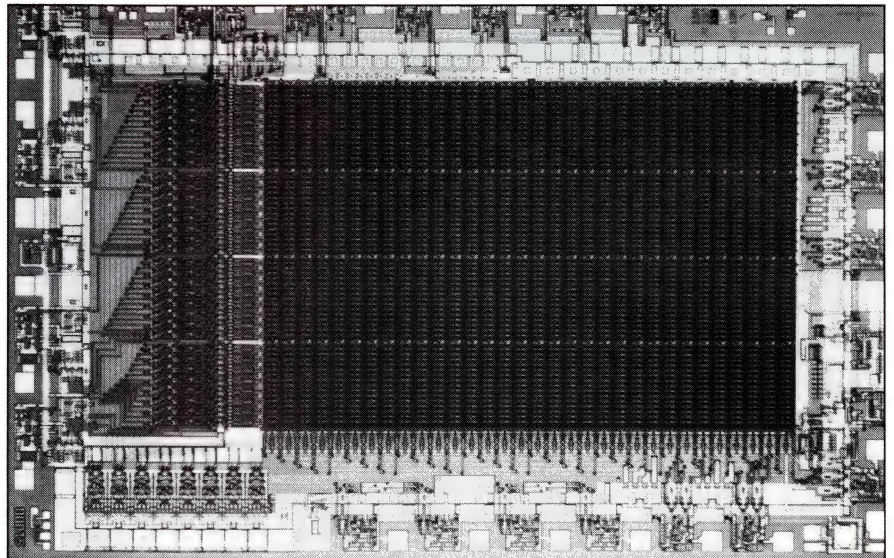
ments of customers is Cirrus Logic Inc. of Milpitas, which is being joined by companies such as VLSI Technology Inc. and Zymos Corp. The newest entry, LSI Logic Corp. of Milpitas, already offers compiler-based products as megacells for semicustom designs and as pinned-out standard products. But now it is forming a semistandard subsidiary, G-2, headed by its cofounder William O'Meara. The first of G-2's semistandard products is a three-chip set aimed at replacing many of the 60 to 80 glue chips that populate the IBM Corp. Personal Computer AT motherboard.

As the digital side of systems speed up, pressure is mounting to eliminate the throughput bottleneck on the analog side. The proposed solutions are roughly comparable to digital developments: higher-speed processes to keep up with speed improvements in the digital side; integrating more of the analog components onto a single chip to reduce interconnection delay; and highly integrated application-specific analog circuits.

The most straightforward way to solve the problem—merging of more analog and digital circuitry onto fewer chips—will continue to prove difficult. The gap between high-performance digital and analog VLSI will continue to widen as digital technology moves below 1 μ m.

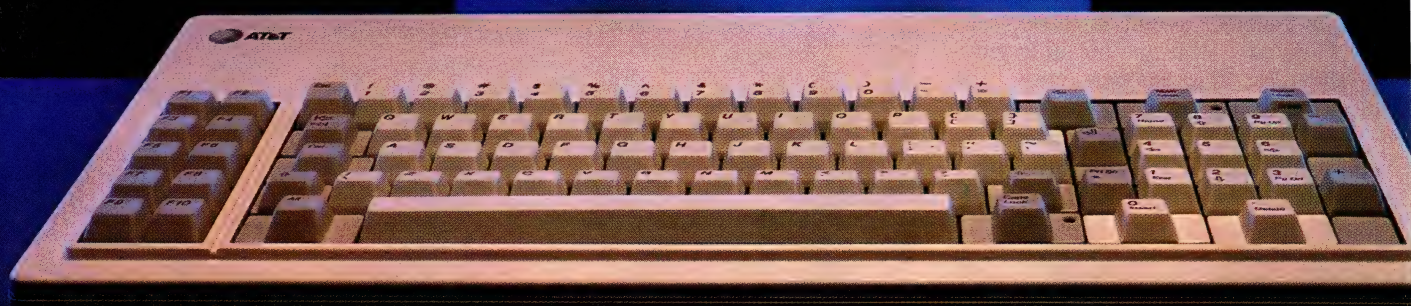
Still, present-generation 2- and 3- μ m analog CMOS processes have allowed designers to bring to chips a level of intelligence and integration not thought possible before, argues Eric Swanson, vice president of technology at Crystal Semiconductor in Austin, Texas. The results are such complex application-specific standard and custom chips as adaptive subscriber circuits and line interfaces for telecommunications, self-calibrating analog-to-digital converters with on-board registers and microcontrollers, and video palette digital-to-analog converters that include on-board RAM. Such high-level analog VLSI solutions will continue to proliferate, he says, even if the level of integration does not go much beyond the present level of 20,000 to 30,000 transistors.

—Bernard C. Cole



MERGED PROCESS. Saratoga Semiconductor's biCMOS 4-Kbit ECL static RAMs embody low power and high speed. Significant density hikes are likely in biCMOS SRAMs in the next year.

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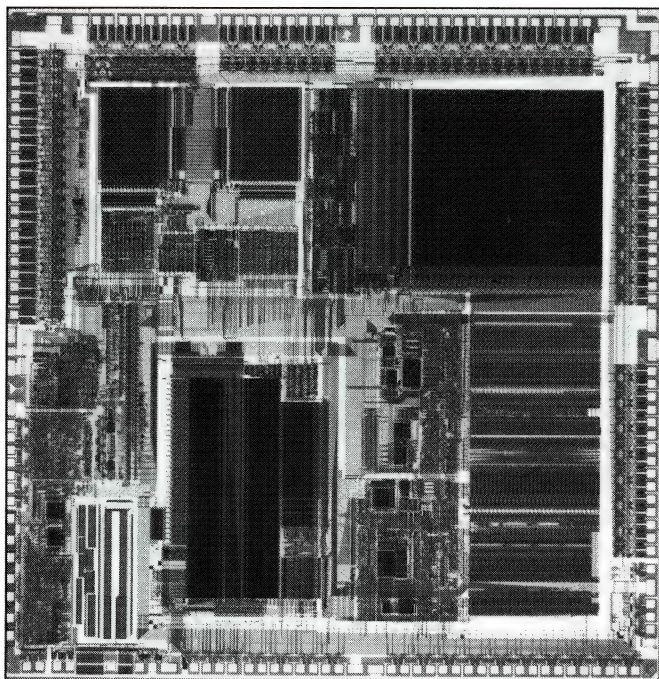
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MICROPROCESSORS

SURPRISINGLY, THEY'RE PROLIFERATING

Standard microprocessor families were supposed to rule in the 32-bit era—but, confounding these expectations, there's a slew of new competition on the way. Microprocessor designers are hard at work on a new generation of algorithm-specific devices to take over many specialized operations from a computer's central processing unit. The software algorithms currently used for such functions don't deliver the performance required when dealing with large volumes of data. Traditionally, this is a problem only for the very largest of supercomputers. But with the development of machines built around 32-bit processors with megabytes of direct-memory access and gigabytes of virtual memory—machines capable of tackling far bigger computing tasks than earlier generations of computers—there is a pressing need for special-purpose algorithms built into the hardware. And as integration levels move toward the ultra large-scale, and as computer-aided design and semicustom methodologies become more sophisticated, it's becoming possible to build them.



FAST SORTER. AMD's content-addressable data manager sorts through data files up to 500 times faster than software-based routines.

Coming Soon

- Algorithm-specific systolic arrays for image, speech, and digital-filter processing.
- RISC chips from big chip makers, all aimed at the standard 32-bit market
- CISC processors that use techniques borrowed from RISC to boost performance

In traditional computer architectures, the first move in this direction was the development of reduced-instruction-set computers and language-specific processors. Algorithm-specific microprocessors are an extension of these concepts. On the numeric side, this means the coming of systolic arrays to perform such tough and time-consuming jobs as image processing, speech processing, and digital filter processing. It also means specialized architectures built for such numerical operations as algebraic computation, linear least-squares calculation, linear programming, and recursive machines.

On the nonnumeric side are a host of tasks that are not well handled by traditional computer designs, but that are prime candidates for special algorithms. Among them are string processing, merging, pattern matching, sorting, text and document processing, searching and sorting, data-base searching and updating, and graph processing.

Indicative of a growing trend is the emergence within recent months of a handful of algorithm-specific products as well as a number of research-and-development efforts within major organizations. In the first category is Advanced Micro Devices Inc.'s content-addressable data manager, which is designed to search and sort through data files up to 500 times faster than software-based sorting routines.

In the R&D arena, increasing attention to algorithm-specific processors is being paid by concerns as diverse as AT&T, General Electric, Hitachi, Massachusetts Institute of Technology, NEC, Nippon Telegraph & Telephone, and Toshiba. For example, at AT&T's Bell Laboratories Speech Processing Department at Murray Hill, N. J., engineers are working on a special-purpose processor optimized for executing graph-searching algorithms. Where a conventional digital signal processor has a central hardware core that can execute kernels of operations such as filtering, signal conditioning, and spectral analysis, a graph-searching processor can also handle such operations as dynamic programming and similarity measurements. All these tasks are important in speech processing, image processing, and artificial intelligence.

At Toshiba's Integrated Circuit Division in Kawasaki, Japan, work is under way on algorithm-specific signal processors for use in speaker-independent isolated speech recognition. Built around a proprietary

pattern-recognition algorithm, the processor is designed to recognize vocabularies that include digits, along with many typical word-processing commands.

Other significant efforts include a compiled chip set for specialized graphics computations from General Electric Co.'s Corporate Research and Development Center in Schenectady, N. Y.; a cosine transform processor from MIT's Lincoln Laboratory in Lexington, Mass.; a pipeline-sorting chip from NTT in Tokyo; and a character string-search processor from NEC Corp., also in Tokyo. All are still in the R&D stage.

In addition, a variety of specialized processors should start to emerge into the marketplace during the coming year. Among the semiconductor makers currently investigating such offerings are AMD, Intel, LSI Logic, National Semiconductor, Texas Instruments, and VLSI Technology. If algorithm-specific devices are still in the toddler stage, RISC microprocessors are maturing into scrappy adolescence. According to Lyle Pittroff, director of strategic development for processor products at AMD in Santa Clara, Calif., a battle royal over RISC is building up in the 32-bit marketplace that will erupt in earnest during the coming year. The opposing forces will be set in motion by the introduction of RISC architectures from a number of semiconductor houses, including AMD, with its Am29000, Intel Corp., and Motorola Inc. A wild card is

the possibility of a second Clipper chip, which may be introduced by the Clipper's new owners, Intergraph Corp., should that company follow the intentions of Clipper's original developers, Fairchild Semiconductor, to keep the chip evolving.

With the addition of these new RISC chips, the 32-bit marketplace will begin to segment itself into a low-to-medium performance range and a high-performance range, with the dividing line at about 8 to 10 million instructions per second, says Paul Chu, manager of product planning at AMD. RISC machines will dominate in applications where performance, rather than compatibility with existing software, is key, he says. Below the dividing line, traditional complex-instruction-set computers based on Intel's 386, National's 32000, and Motorola's 68000, will continue to dominate, he predicts.

However, says Chu, the CISC machines of tomorrow will in many respects bear more relationship to their RISC competitors than to their earlier CISC predecessors. "In order to squeeze as much performance out of their designs as possible, the new CISC machines will incorporate features, such as on-chip cache, that are traditionally associated with RISC machines," he says. "However, in the most important areas, such as instruction complexity and the number of machine cycles to execute an instruction, there will continue to be a wide gulf."

—Bernard C. Cole

CAD/CAE

NEW TOOLS WILL BREAK DESIGN BOTTLENECKS

As pervasive as it is becoming, computer-aided design and engineering is still hobbled by several problems. But help is on the way, and a growing number of solutions will become available in products next year. Design tools that are emerging are smarter, able to handle analog as well as digital signals, and can help speed up the development of test programs.

New tools will be able to tell designers how to improve a design before it gets implemented in silicon or on a printed-circuit board. Some design tools are beginning to take advantage of artificial intelligence—they predict die size and power consumption; others automatically reduce the amount of logic in a circuit at the schematic entry stage of design. Expert systems will also critique a schematic and netlist, telling the designer where the circuit can be improved.

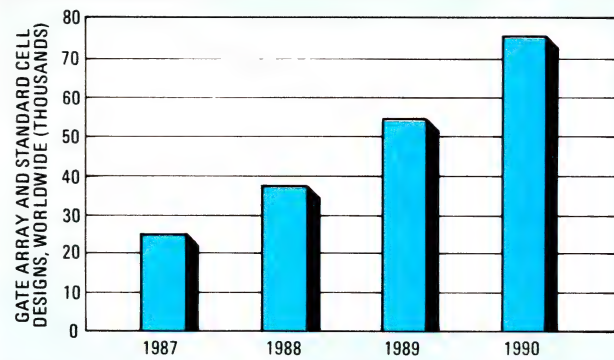
Coming Soon

- Interactive adviser tools that will help to optimize designs before implementation
- Analog and mixed-signal simulators to break a major bottleneck in system design
- On-chip circuits for testing all of the nodes on complex application-specific ICs
- New tools that eliminate the need for or speed up exhaustive fault simulation

New simulators for analog circuits and mixed-signal simulators that test both analog and digital circuits will become more common and more capable. They will help break one bottleneck in total system design: analog-circuit simulation. The new analog simulators will provide the reliability and accuracy lacking in the Spice simulator, the public-domain package that by default has become virtually a standard for analog design. And they will enable higher-level behavioral models of analog circuits just as there already are for digital. This is especially critical now because of the plethora of new designs containing analog circuits. Similarly, the new mixed-signal simulators will handle the designs that combine analog and digital circuitry.

CAE tools are also coming that should help break another serious bottleneck in the overall design process: the difficulty in producing test programs as

ASICs ARE RAMPING UP



SOURCE: TECHNOLOGY RESEARCH GROUP

quickly as new circuits are designed. New simulator algorithms will allow fault simulation 100 times faster than is possible with the current generation of fault simulators. And new software tools may be in the offing that eliminate the need to perform exhaustive fault simulation at all.

There is a compelling reason why design tools have to improve in these three ways: the exploding number of application-specific integrated circuits. ASICs are getting much larger and correspondingly complex—they will be growing to 50,000 gates in the near future, compared with the 20,000-gate designs of today. And besides getting bigger, there are going to be a lot more of them.

More than 76,000 merchant-market ASIC designs will be completed in 1990, three times more than the 25,379 completed in 1986, predicts Cindy Thames, vice president at the Technology Research Group, a market-research firm based in Boston. In addition, she says, the number of new pc-board designs is also growing. They're also larger, more complex, and more likely than single chips to include significant mixing of analog and digital circuitry. Some 900,000 pc-board designs will be completed in 1990, 50% more than the 635,000 done in 1986.

To cope with the increased number of new designs, the designer will be able to rely on smart tool kits that can give him expert advice. Today, there are tools that inform designers about the amount of power a design will draw, the number of pins it will need, and the size of the final die. The next generation of these tools will be represented by the new Design Assistant coming in the first quarter of 1988 from VLSI Technology Inc. of San Jose, Calif.

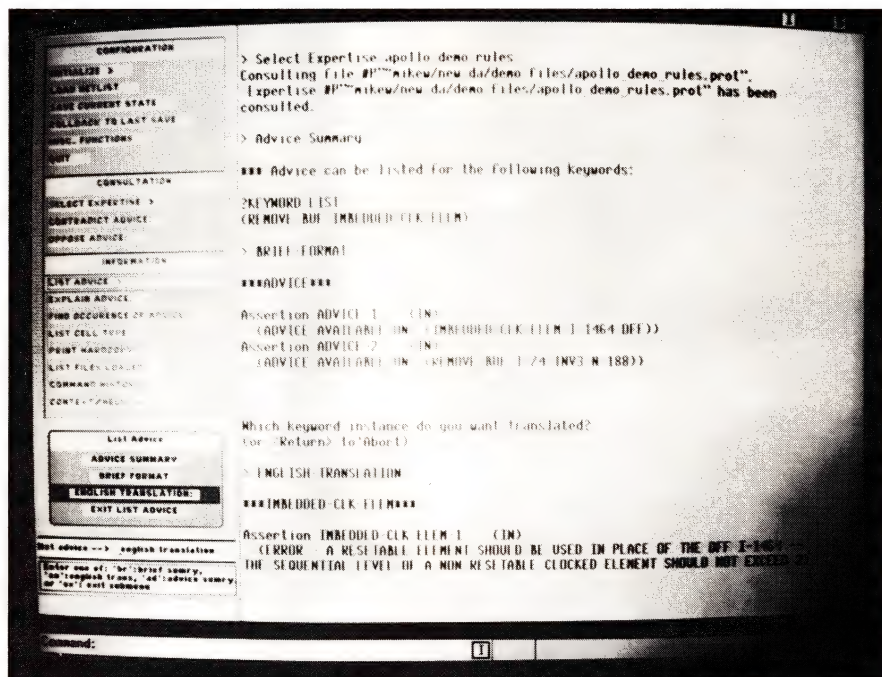
The new version of Design Assistant essentially can work with whatever information the designer gives it. Knowing only the number of gates, it can provide a rough de-

sign that will come within 20% of the actual size of the final chip, says Daniel Skilken, the company's product marketing manager. Working from a schematic, it will come up with a design that is within 1% of the actual size, power consumption, and number of pins necessary to handle that power. Given the chip layout, its accuracy will be total. Up to now, such tools could provide only rough estimates of die size.

And increasingly the tools that estimate die sizes will be interactive, allowing the designer to hone his work with more and more input, says David Hightower, manager of advanced IC systems at the Calma Company in Milpitas, Calif. "The designer supplies the software parameters describing the number of gates in the design, the expected occupancy—80%, for example—the expected logic type—purely combinational logic, mixed combinational and sequential, or totally sequential—and the expected completion rate—99.9%, and so on." With each input, the tool makes a prediction; as it gets new input or changes to earlier input, it refines its prediction. The designer keeps adding and changing input until eventually the tool hits the desired die size.

Hightower says this type of tool will allow the designer to specify the size of one side of the device and the tool will adjust the other to accommodate the layout. Or he can let the tool pick the size of both sides and try to minimize the total size of the gate array. Finally, the designer supplies the tool a route constant, which is a measure of how difficult it is to route this particular structure. "With this kind of information, a software tool can very accurately estimate final chip size," Hightower says. In fact, Calma is planning just such an addition to its EDS III tool kit [*Electronics*, Sept. 17, 1987, p. 92] in 1988.

Besides advice on the physical packaging of a design, designers can expect better advice on how to



HELPFUL. The Design Adviser, an expert system from NCR Corp., responds to a user's request by suggesting a direct reset line to make an embedded clock element more testable.

improve their overall designs. The Design Adviser [*Electronics*, June 25, 1987, p. 31], an expert system from NCR Corp. of Ft. Collins, Colo., provides specific counsel on improving performance, testability, and manufacturing yield.

Next year, designers can expect to see competitive packages and enhancements for the current capability. "Designers can expect to have software to suggest better ways to simulate their circuit," says Robin L. Steele, NCR's senior principal engineer for the product. "For example, certain state machines should be simulated on both edges of a clock to determine if problems are created when the clock shifts phases."

The industry can also expect tools to provide advice on better implementation of circuit function. But the job of the tool suppliers will be difficult, because the kind of expert system needed to advise on how to make a better circuit function faces the problem of understanding what a circuit is supposed to do, working only from the information it can derive from a netlist. "For example, software can be written that can analyze a circuit and recognize a bank of flip-flops and NAND gates and deduce from this that it has come upon a counter," says Steele. "But what kind of counter is it—a ripple counter, an up/down counter?"

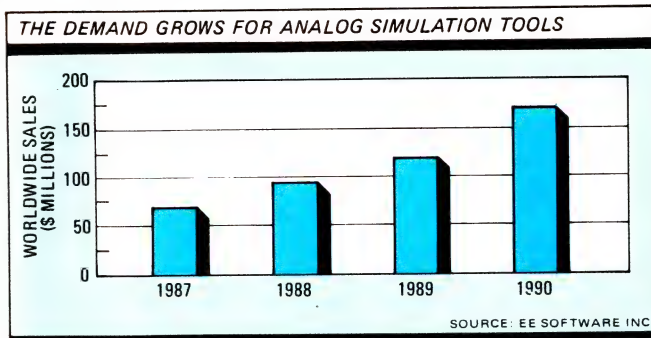
NEW SOFTWARE IS NEEDED

The software can't make this kind of decision by examining connectivity and circuit components. "New heuristics need to be developed to help make this determination," Steele says. "We could ask the designer to explain to the software what kind of counter it is, but we're trying to minimize the amount of work the designer must perform to achieve the analysis. The other side of this problem, of course, is that if you ask the designer, he may be mistaken, so it is best for the tool to extract the information itself."

Projects are under way at NCR to develop expert systems that can help devise a heuristic procedure for partitioning a design in preplanning a layout. One such project at NCR may be combined with the Design Adviser, according to Daniel Ellsworth, NCR's manager of advanced development strategy. "With each new generation of tools and process technology there is a limit where the state of the art in tools breaks down, and a large design has to be broken down into smaller units that the tools can handle," Ellsworth says. "That is when a tool to improve partitioning becomes important."

Performance evaluation and improvement is another aspect of the design process needing expert help. Already available is the capability of making speed and area tradeoffs for buffering and excessive fan-out. This capability draws on a technique called logic-chain analysis and local transformation, in which the tool analyzes a collection of logic circuits—a logic chain—and suggests changes to them—a local transformation—that improve their design. For example, it might tell the designer a gate in the design might need higher output current drivers to provide a better signal level to the gates it drives.

Tools to perform logic minimization are available from companies such as Optimal Solutions Inc., the



General Electric Co. spinoff in Research Triangle Park, N. C., and VLSI Technologies. Future generations of tools, however, will be more extensive in their capability. They will probably resemble the intelligent compiler introduced by Silicon Compiler Systems Corp. of San Jose, Calif. [*Electronics*, April 30, 1987, p. 54]. "While logic-minimization tools attempt to optimize a design for one of two variables (speed and area), an intelligent tool will optimize a design for functional, performance, and physical-layout constraints set by the designer," says Philip Kaufman, chairman and chief executive officer at SCSC.

While tool suppliers have been raising the intelligence of tools to perform digital design, they have not built equally powerful tools—especially analog simulators—for mixed analog and digital circuit design. By 1990, 39% of semicustom designs will have analog functions, according to Cindy Thames at the Technology Research Group. Moreover, the analog simulation market is no small niche either. The total analog simulation market for 1987 will be about \$65 million, with projected growth to \$80 million in 1988, \$120 million in 1989, \$170 million in 1990, and \$210 million in 1991, says Kevin Walsh, vice president of marketing at Electrical Engineering Software, a San Jose, Calif., company that offers an analog simulator. Furthermore, he says that only 10% of CAE work stations are currently using analog design tools.

"The product everyone in this market is waiting for is a true mixed-signal analog and digital simulator," says Walsh. Most tools for mixed circuits actually use dual simulators. For example, Viewlogic Systems Inc. of Marlboro, Mass., uses its own 28-state logic simulator, Viewsim, to perform digital simulation, and uses the PSpice analog simulator from MicroSim Corp. of Laguna Hills, Calif., to simulate analog components. The two tools work concurrently. Sierra Semiconductor Corp. of San Jose, Calif., was heralded as having the first behavioral simulator to allow both analog and digital functions on an IC to be simulated together [*Electronics*, October 16, 1986, p. 60].

"The problem with mixed-signal simulation is that it combines a logic simulator with a Spice simulator," says Prabhu Goel, president and chief executive officer of Gateway Design Automation Corp. of Westford, Mass. "Spice is too slow to perform significant mixed-mode simulation." The limited mixed-mode simulation today cannot handle components more complex than digital-to-analog converter, analog-to-digital converters, operational amplifiers, comparators, and

so on. Moreover, today's mixed-mode simulators cannot handle closed feedback loops involving only analog components. Goel believes that the required solution is an analog simulator that provides behavioral- and transistor-level analog models somehow married to a good logic simulator. One company which already has such an analog simulator, called Saber, is Analoggy Inc. of Beaverton, Ore. [*Electronics*, Oct. 30, 1986, p. 80]. "Saber is the first analog simulator with full-time domain modeling," says Larry Jacobs, president of the company. "This capability is a requisite for building a true mixed analog-digital simulator."

Besides being able to perform true mixed analog and digital simulation, another bottleneck is the difficulty in rapidly creating test programs for designs going into production. The obvious solution is to improve the design-to-test link. But for very complex ASICs and pc boards, the availability of the designer's test patterns does not guarantee that a manufacturing test can be developed to find every possible error condition for a chip or board. The next two years should see the advent of solutions to this problem.

One solution being considered is adding special circuits to an ASIC device to guarantee that every node in the chip can "toggle"—change from 1 to 0 and back. Another solution creates the test patterns needed to test a chip or board, but it encourages the addition of scan-path circuits in the designs.

One man who makes a case for the first alternative is John Conover, director of engineering at SMOS Systems Inc., an ASIC foundry in San Jose, Calif. "One way of automatically increasing fault coverage is to use a cross-checking technique," he says. The cross-checking scheme resembles an x - y matrix overlaid on the interconnect layers of an ASIC. Nodes fall on junctions of the matrix's x and y intercepts. A tester can

address every node on the chip by selecting the correct x and y lines of the matrix. By monitoring each node while the logic simulator's stimulus patterns are applied to the chip's input/output pins, the tester can determine that the node changed in response to an input stimulus. Without some way of monitoring nodes inside the chip, the test engineer must write stimulus patterns that produce responses on the chip's input/output pins, indicating that each node inside the chip changes states.

"We experimented with the scheme and found that adding the testability circuits increases die size by around 5%," Conover says. "The big advantage, however, to this technique is that there is no need to run a fault simulation because the tester can address any node on the chip." This is no small advantage on devices with over 20,000 gates, where writing test patterns to toggle every node can take a lot of time.

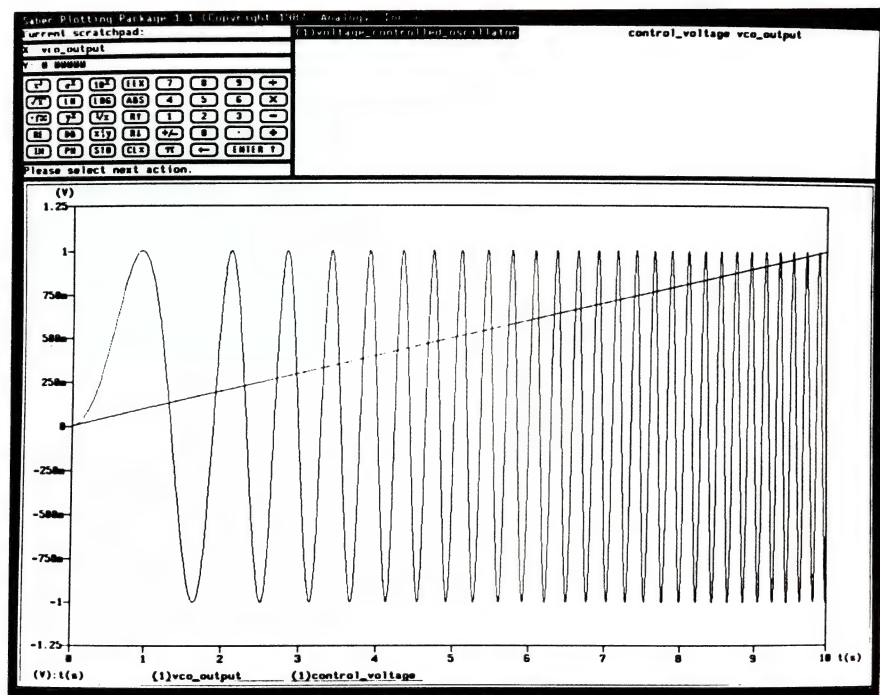
Critics of this approach charge that toggling nodes are not true indicators that a circuit is functionally operational. To detect a failure at a node, Goel believes, the test system must be able to determine that a pulse condition on one node can propagate to some point farther along in a signal path. Scan paths reduce the complexity of test-pattern development and cut back the computer time required to perform complete fault simulations. In addition, "they automate some test-vector generation inside of the chip to provide fault coverage above 90% with no additional requirement of the designer," Goel explains. "To achieve this fault coverage, the designer has to give up between 4% and 20% of the chip area."

Fault simulation has made a major leap forward in adopting a probabilistic algorithm, a trend that bodes well. There are three types of fault-simulator algorithms common in use today: deterministic, statistical, and probabilistic.

The first is the most thorough, but also the most compute-intensive. The second cuts compute time significantly but does not provide the accuracy of the deterministic method.

The newer probabilistic algorithm is based on the so-called Stefan Algorithm. Companies now offering this algorithm are Gateway Designs and Caedent Corp. of Colorado Springs, Colo., which Mentor Graphics Corp. of Beaverton, Ore. purchased. These new fault simulators execute 100 times faster than a deterministic algorithm, yet are within 2% of the accuracy of a deterministic algorithm. And, unlike a deterministic simulator, which tells a designer only the percentage of the nodes tested, a probabilistic-based simulator also tells the designer where in the design he can find the untested nodes, so that he can create more patterns that will test them.

—Jonah McLeod

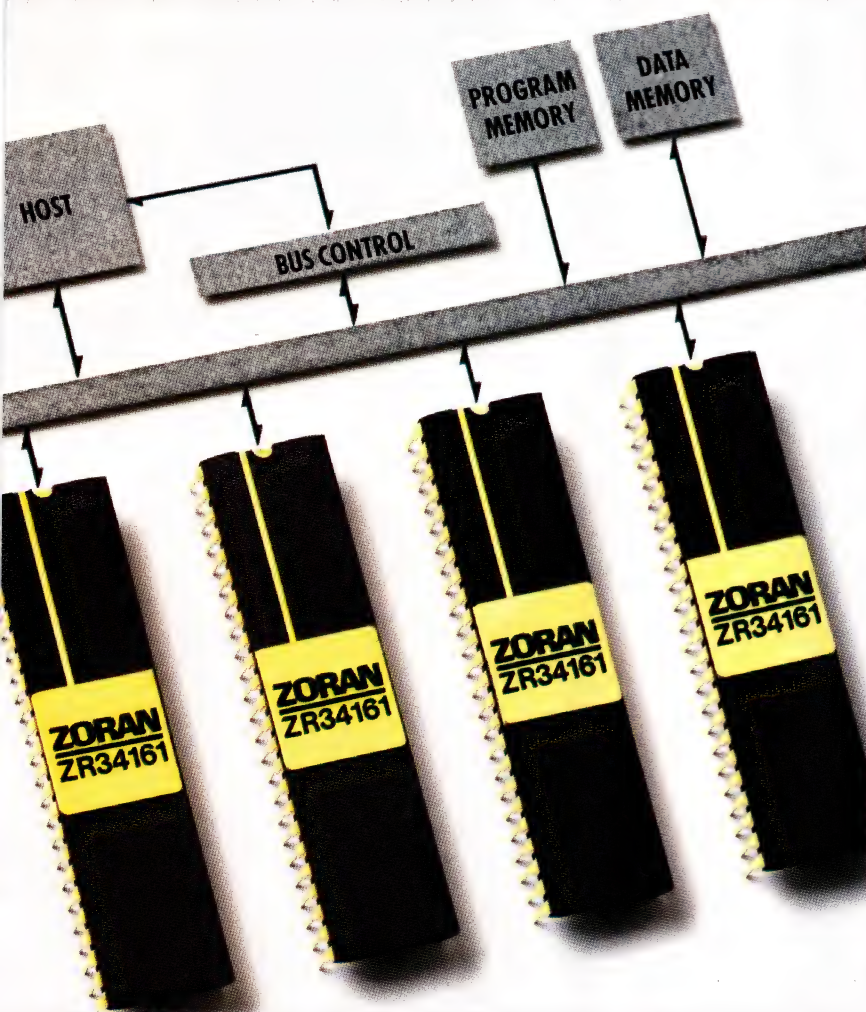


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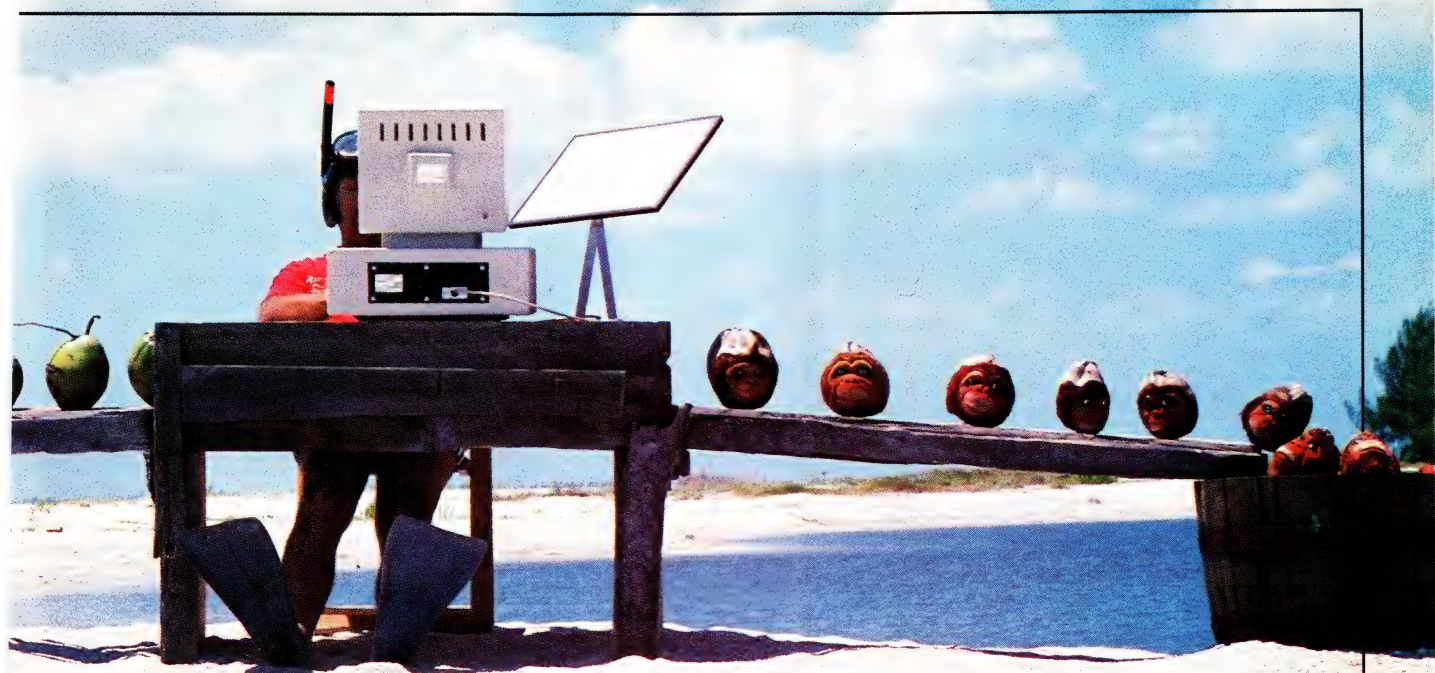
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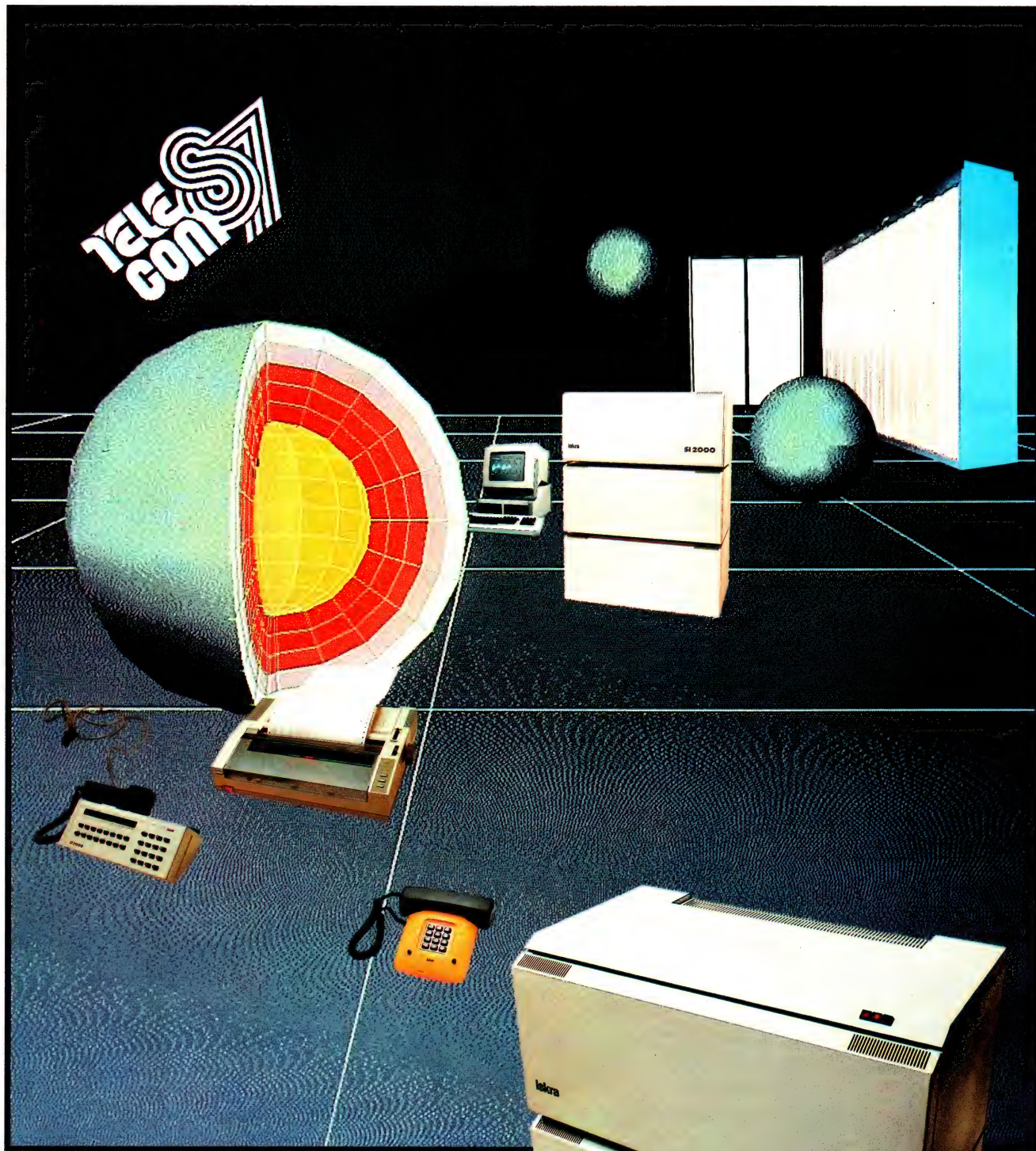
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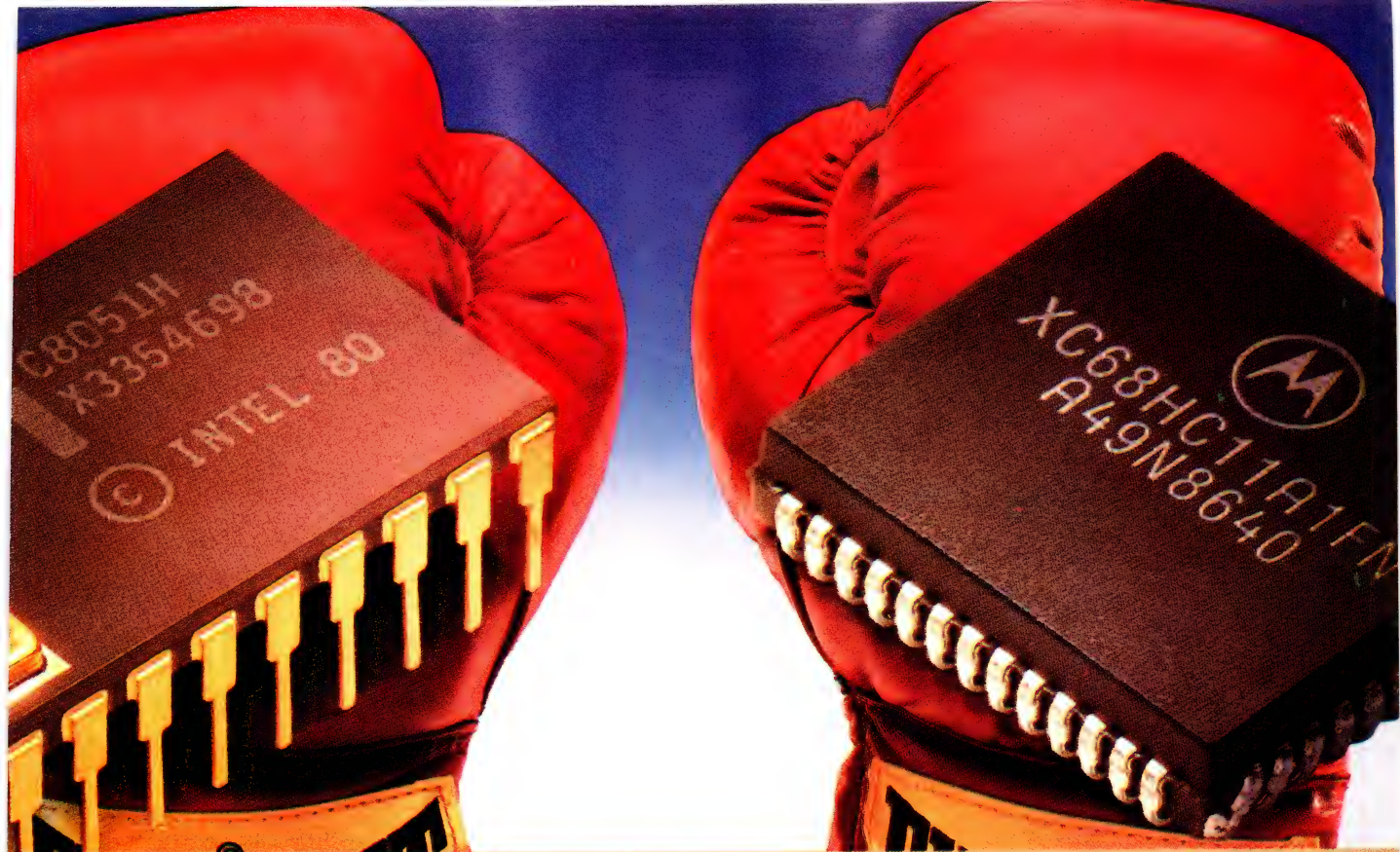
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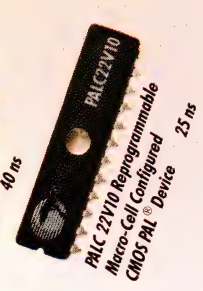
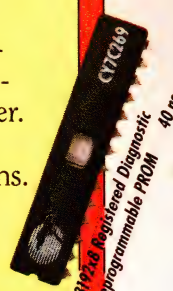
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TEST & MEASUREMENT

THE DIGITAL TAKEOVER PICKS UP SPEED

In test and measuring equipment, changes aren't as sweeping as those shaping semiconductors and computers. But the factors that affect instruments are numerous and complex, and the results, although taking longer to arrive, are no less dramatic.

Changing technology is one key force, most notably in the inexorable shift to digital instruments. Changing test requirements are another crucial factor, one affecting every application area. In fields ranging from research, design, and development to manufacturing, engineers are turning to computer-automated testing and to automated measurements so they can handle the voluminous data being generated.

There is a growing demand in almost all testing segments for greater functionality, ease of use, and increased modularity. This move is feeding a drive for standardization, at least in buses, as the capabilities of test and measurement equipment diversify: more and more functionality is being added, and at the same time ATE gear is becoming more narrowly focused, growing more application-specific.

If there is one word that touches all test bases, it is "digital." All the classical measuring instruments—oscilloscopes, multimeters, signal sources—went digital long ago. Analog instruments still dominate in sheer numbers, offer the best performance in most measuring categories, and carry lower price tags, but that will soon change. Galin Wampeter, president of Prime Data, a market-research firm in San Jose, Calif., says that sales of digital scopes, for example, are growing at a 22% rate, compared with only 2% for analog and 10% for instruments in general. By 1991, digital scopes will hold the larger share of the market for the first time (see chart). Digital performance is gaining, too. The analog scope is holding at 1-GHz best bandwidth; the digital version has hit 20 GHz, and keeps climbing.

The shift to digital is caught up in the movement toward computer-aided engineering and manufacturing.

Coming Soon

- A lot more digital instruments, including oscilloscopes with bandwidths better than 20 GHz
- Tools that can test chips and boards, as well as systems that link engineering to manufacturing
- Computer-aided testers that can find faults in designs, components, or processes

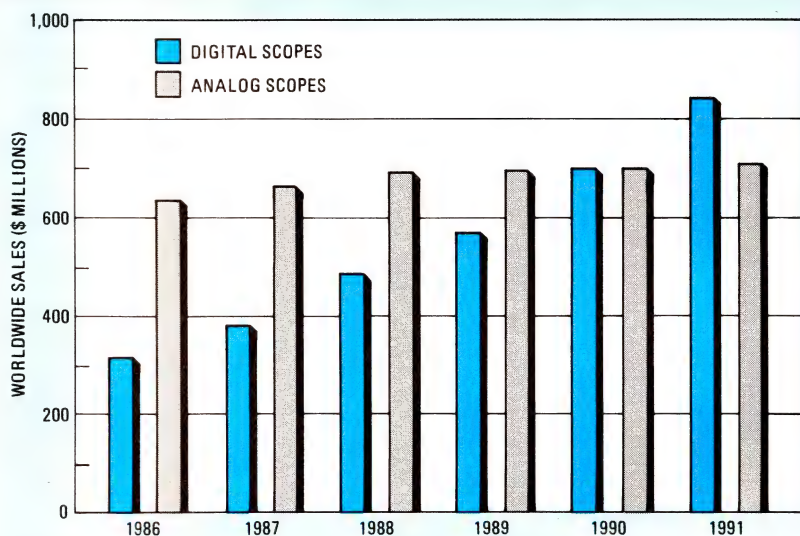
Engineers working on CAE systems need to simulate and verify their designs. For that purpose, digital instrumentation is a natural. Reduced to essentials, CAE designs are little more than logic 1s and 0s—fodder for equipment like the new Tektronix DAS 9200 digital analysis system or Hewlett-Packard Co.'s 16500A logic analysis system. Both of these can tackle chips, boards, or systems, and both can close the design loop, linking engineering and manufacturing.

The net benefit of such digital instrumentation is productivity. Design time gets shorter. The first design works—at least, that's the

goal—so chips and boards get to manufacturing sooner. With CAE-to-ATE links, products get tested better and faster. Better-quality products reach the market faster and cost less.

The push to digital is related to the equally strong drive for computer-aided testing, a subset of computer-integrated manufacturing. "Manufacturing is the hottest test area today, with the greatest needs and the biggest shifts," says Frank Hermance, general manager for laboratory instruments at Tektronix Inc. in Beaverton, Ore. And that's particularly true in the U.S., says John Battin, president and chief operating officer of

DIGITAL OSCILLOSCOPES ARE TAKING OVER



SOURCE: PRIME DATA

Wavetek in San Diego, Calif. There is a driving force to get quality and yields up and that is changing the test equipment going into factories, he says.

Computer-aided testing, or CAT, combines instruments in various forms—modular, rack-and-stack, on-a-card—with computer hardware, including displays, keyboards, peripherals, input/output devices, and the like, plus software—operating systems, networking, graphics, windows, libraries, applications, and so on. The target is to find faults in design, components, or manufacturing, the major offender in the shipping of defective products. CAT's payoff is simple: potentially huge savings in costs that can be passed on to the customer, with enough left over to provide a comfortable profit margin.

To a vendor, then, CAT can mean survival in the world marketplace; to a customer, it means a better-quality, affordable product. Says Ned Barnholt, general manager of Hewlett-Packard's electronic instruments group: "The way to reduce costs and improve manufacturing productivity is by improving quality, eliminating scrap and rework, getting it to work the first time. To do that calls for information and measurements—about what is happening out there on the production floor, the quality levels, the yields, the specification margins. Only then can better decisions be made on how to reduce costs. CAT as part of a CIM network will automate those measurements, provide the front-end data collection that can be fed back to an information-management system on a factory floor."

Barnholt says that users not only want easily integrated instruments with high measurement throughput, but those that can be tailored for specific applications. Two ways to do that, he says, are with software

and modularity. He predicts more powerful software tailored for the job, as does Bill Terry, executive vice president for HP's measurement-systems sector. "Engineers want application software for test automation," Terry says. "Even though they now have higher-level languages, they find test-automation tools still too hard to use."

Terry sees modularity as one way of satisfying requests for more functionality, especially among the military and its prime contractors. "People want modular instruments because they perceive they can spend less and get smaller instruments. Our job is to meet those perceived needs, but sometimes it's a little tough because modularity doesn't always save money—it can cost more."

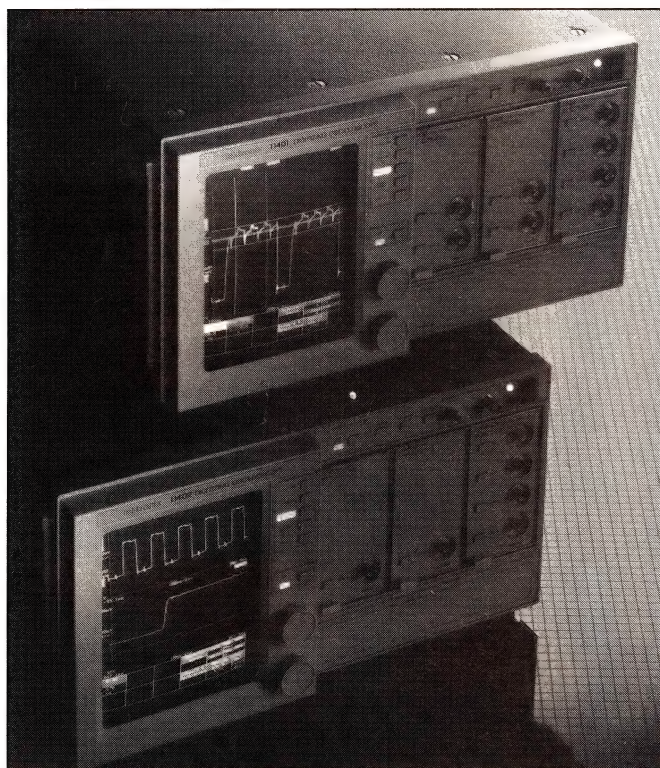
A MODULAR STANDARD

Nevertheless, modularity can offer standardization—something universally desired these days—and HP has teamed up with Tektronix, Wavetek, Racal-Dana Instruments, and Colorado Data Systems to propose a modular standard for instruments on a card. Based on a VMEbus extension called the VXibus, the proposed standard is now under consideration by an IEEE committee. It will establish protocols, interconnections, a backplane and chassis, and printed-circuit-board design for the VXibus.

Tektronix's Hermance sees the VXibus as the answer to the limitations of the GPIB standard with respect to speed and the number of instruments accommodated. But Terry emphatically states that the GPIB will not die. It has some deficiencies, he admits, but thinks those could be cured through an evolutionary standards process. He delineates the differences between the origins of the two buses: GPIB "was a self-invented HP contribution. We didn't go out and do a lot of work with users on whether they thought it was a good idea. We invented it, sprung it on the world, and people said, 'boy, that's a good idea.' That is not how VXibus got started, though. Users said, 'we want instruments on a card and a standardized backplane. Why not start with VME? That's as good as anything. Industry leaders said, 'We hear you. We'd better get cracking here.'"

The future of the VXibus probably depends on whether or not it emerges as an IEEE standard. Wavetek's Battin predicts that "the VXibus will happen, but more slowly than some people would expect. An IEEE-approved standard takes more than a few weeks, and you never know what questions they will come up with." Prime Data's Wampeter states flatly: "Within 10 years, instruments on a card will hold 20% of the market, but GPIB-based systems will reserve a place by interfacing to VXibus subsystems."

If modularity doesn't save money, it does let users put together lots of functions under one roof. Instrument vendors have been doing that for some time in stand-alone benchtop and other equipment, but the effort is escalating as "functionality" becomes the watchword in the customer's test lexicon. One of the best recent examples is the Tektronix 11000-series analog and digitizing oscilloscopes, members of which include counter-timers, display up to eight channels of

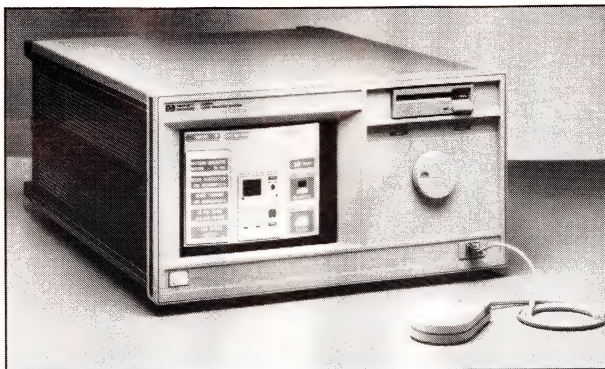


DIGITAL TAKEOVER. Digitizing scopes, like the 11000 family from Tektronix, are destined to become the workhorse of the future.

information, and make highly accurate frequency and time measurements not usually expected of oscilloscopes. Another trendsetter, HP's 16500A logic analysis system, attacks digital measurements with up to 400 general-purpose channels and 80 1-GHz timing channels, backed by a 204-channel, 50-Mbit/s pattern generator and an 8-channel 400-Msample/s digitizing oscilloscope.

With all this firepower, one would expect front panels bristling with buttons and knobs. Yet both the HP and Tektronix boxes are surprisingly bare of controls. Instead, Tektronix has gone to touch screens, pop-up menus and icons, and to nondedicated spin knobs, which change personality at a user's request and so control more than one instrument parameter. HP has done the same in its analysis system and thrown in color displays to boot.

In fact, the human interface is receiving considerable attention industry wide. Internal microprocessors, chip memories, software and "soft" keys, digital functions, touch technology, and other new techniques are all teaming up to replace the old hard-wired controls and buttons.



FUTURE TOUCH. The simple front panels and touch screens on HP's 16500A logic-analysis system are instruments' new look.

When a test-equipment vendor adds functionality, he is really taking a step toward greater specificity. In the last few years, those making measurements or involved in product testing have pushed for turnkey solutions, equipment dedicated to specific test tasks. By and large, vendors have responded. Communications gear, memories, power supplies, operational amplifiers, and other analog functions, for example, all have

dedicated testers, and that trend will continue.

But specificity poses a problem for vendors, who would like to reach as wide an audience as possible with a particular test product. Especially with CAT systems, for which vendors must address the issue of which platform or which operating system to adapt, a vendor must decide which level of functionality to provide. That is, should the system be a set of tools, with which the user shapes his exact testing needs, or should it be a complete turnkey product? Hermance says that Tektronix is moving toward partial applications solutions, those that are not full turnkey systems. Others are doing the same, as instrument watchers in 1988 will confirm.

—Stan Runyon

CONSUMER

AT LAST, THE TV PICTURE GETS SHARPER

New technology will hit the consumer-electronics marketplace next year, in the form of visibly improved TV receivers and video cassette recorders. And digital audio tape equipment is likely to start appearing in the U.S. whether or not the controversy over copying prerecorded material is resolved.

Japan is marching steadily along toward its vision of high-definition TV, taking carefully planned intermediate steps, and has proposed a format for HDTV as an international standard. HDTV is several years away, but the first moves will be to new types of digital TV sets compatible with current broadcast standards but providing a higher-resolution, clearer picture. These sets should hit Japanese and U.S. markets next year.

In the U.S., the National Association of Broadcasters will be working next year on techniques that could be

Coming Soon

- The first improved-definition TV receivers, which claim up to 40% better resolution
- A "super" home-video format producing better images than most professional systems

used to broadcast HDTV signals like those proposed by Japan, signals which do not fit in a standard 6-MHz-wide TV channel. But the U.S. is not ready to settle on an HDTV standard; consideration will be given, for example, to a competing proposal recently made by General Electric Co.'s NBC and RCA subsidiaries. There is resistance to the Japanese HDTV standard proposal in Europe, as well, primarily from set makers who fear further Japanese inroads.

The Japanese, however, aren't waiting for the standards-making process to catch up with technology: they want to find outlets for the better TV sets, VCRs, and cameras they now know how to make. They are building equipment for new formats that will allow home-video buffs to make recordings with resolution and quality superior to the tapes made by most professional video systems.

Japanese and European builders of audio equipment



WE NEED SPACE. The National Association of Broadcasters demonstrates high-definition TV to Congress, pointing out that HDTV signals do not fit into current 6-MHz channels.

are also pushing ahead with plans for digital-audio-tape products. But DAT faces legal obstacles in the U.S.: Congress has a bill before it that would force DAT-equipment makers to install a chip to prevent users from making copies of prerecorded material. The bill is expected to come to a vote before the end of the year.

The two intermediate steps that the Japanese have planned leading up to HDTV are called Improved-Definition TV and Enhanced-Definition TV. IDTV is almost here, however: set makers may have IDTV sets on the market as soon as next year, and since they work from the signal now standard in both countries, they should appear in the U.S. soon afterward. EDTV broadcasts are scheduled to begin in Japan in 1989, but may not be implemented outside of that nation.

IDTV uses digital techniques—field memories and motion-detection and image-processing circuits, for example—to improve picture quality substantially, boosting resolution by 30% to 40% and implementing 60-Hz noninterlaced scanning on the screen. It offers cleaner color, enhanced outlines within the image, and fixes defects like interline flicker and dot crawl. NEC Corp. is starting to market chip sets and has shown a prototype TV, so competitors won't be far behind.

The world outside Japan may ignore EDTV, which boosts picture quality even more than IDTV through a new broadcast standard compatible with current TV sets and channel allocations. But U.S. and European standards makers are working on the big jump, anticipated for the early to mid 1990s: the move to HDTV, or something like it. HDTV as defined in Japan is incompatible with the current standards. So it requires new sets and new broadcast equipment—and it will require new channel allocations because no way has been found to fit the signal into a 6-MHz TV-channel slot.

The Japan Broadcasting Co. (NHK) has defined a format with 1,125 scan lines and an aspect ratio wider for a given height than the current standard. The International Radio Consultative Committee is considering a proposal for its use as a studio-recording standard, but it hasn't been accepted yet even at that level.

In the U.S., NAB has set up the Advanced Television

Systems Committee in Washington, D.C., to develop an advanced-TV standard suitable for delivery over all media, including cable, satellite, and terrestrial broadcast, says its director, Benjamin Crutchfield. The big problem is availability of spectrum space for terrestrial broadcasts. NAB sees uhf as the most logical place for HDTV, if that is to be the new standard, so it has been lobbying at the Federal Communications Commission to prevent allocation of uhf space to land-mobile uses. The FCC has issued a Notice of Inquiry on Advanced TV Systems to look at a variety of methods for improving TV pictures, including HDTV.

NAB demonstrated HDTV to Congress earlier this year in an experimental broadcast that used the sig-

nal-compression technique developed by NHK, a system called MUSE (multiple sub-Nyquist sampling encoding). MUSE is considered the most advanced but requires 8 MHz of bandwidth. This month the NAB will begin tests of broadcast techniques that split the signal into two so that existing channel allocations can be used for HDTV. This causes some sticky problems, such as selective fading and timing differences between the two channels. Crutchfield expects these tests to take about a year. "Then we'll move into conducting tests of specific HDTV systems," with broadcasting tests beginning in 1989, he says.

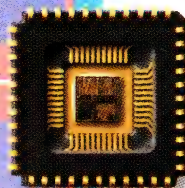
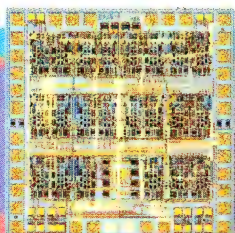
The FCC's Notice of Inquiry has just smoked NBC's entry out of the secrecy of the lab. NBC calls it Advanced Compatible TV; it is to have 1,050 scan lines, a 25% wider screen, and a broadcast signal compatible with existing sets. Furthermore, NBC claims its system will work within the 6-MHz channels now used, although the system has not been proven in the field. The system has only been simulated, despite \$45 million spent by NBC over a 10-year development period. NBC promises demonstrations and progress reports soon.

Self-contained video-recording systems, including cameras, VCRs, and monitors, need not wait for new broadcast standards. JVC, Matsushita, Hitachi, and Sharp have adopted an improved format for such systems, called SVHS, that boosts scan-line resolution about 60% over VHS VCRs. SVHS is expected to stimulate the market for larger picture tubes, with diagonal measurements of 30 or 40 in. Sony Corp., has developed a Beta format with even higher resolution and has built a 45-in. picture tube.

Sony is also jumping into the DAT market—in Europe and Japan, at least—with a portable machine, starting in December. Matsushita, too, has announced plans to start marketing a portable-DAT system in Japan in November. And one U.S. company, Marantz Co. of Chatsworth, Calif., says it will enter the U.S. market with a DAT machine early next year despite the anticopying controversy.

—Jeremy Young
Additional reporting by Charles L. Cohen and Wesley R. Iversen

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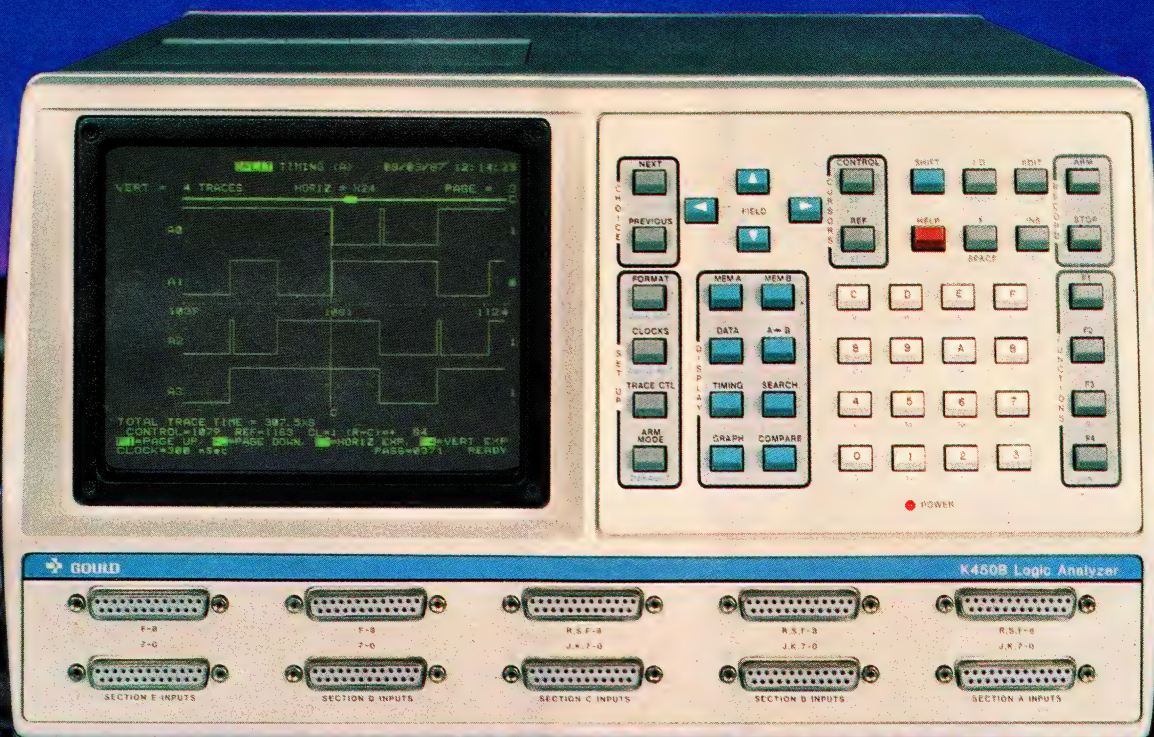
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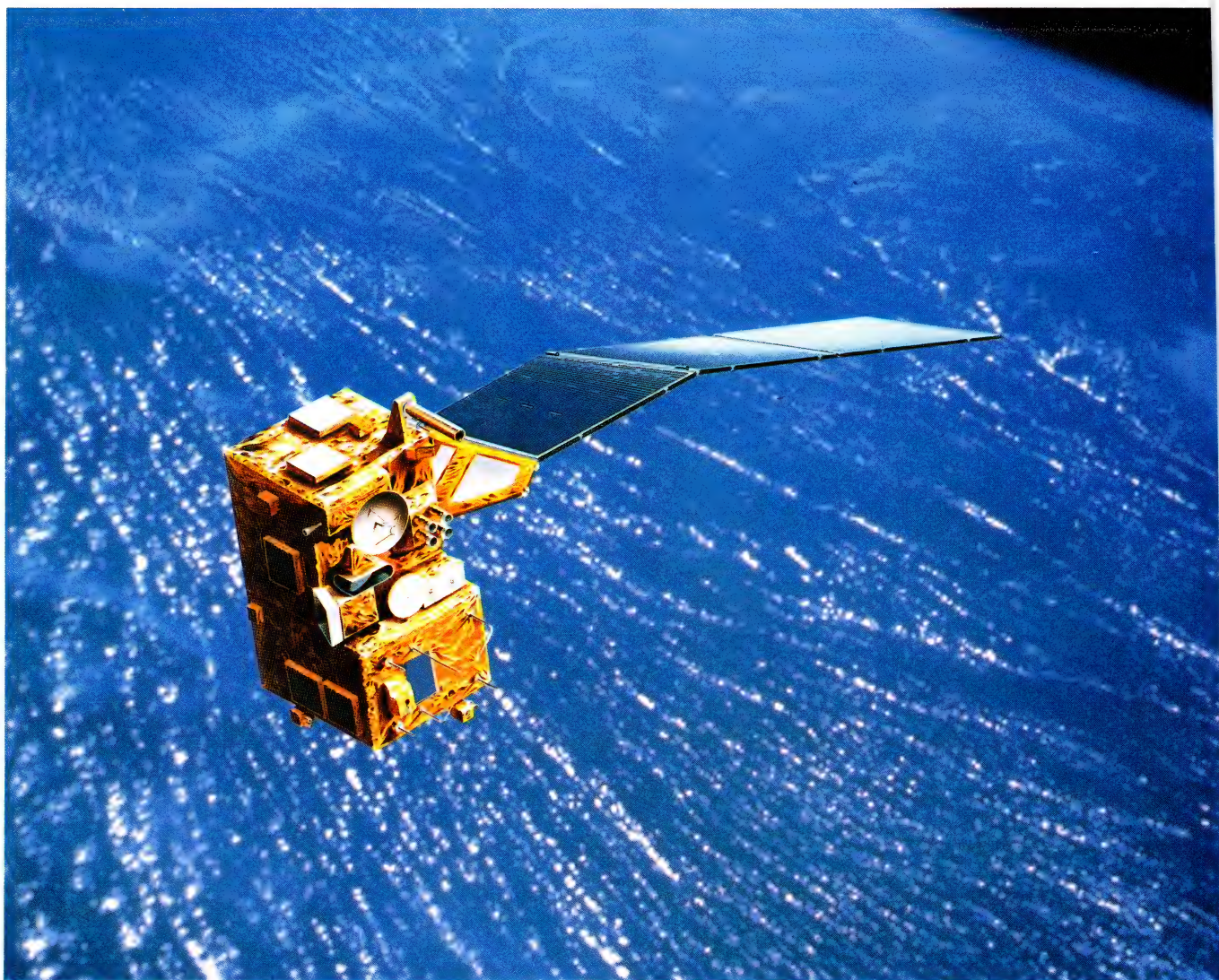
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JAPAN LAUNCHES INTO A NEW ERA IN REMOTE SENSING.

Japan's first Marine Observation Satellite-1 (MOS-1) is now circling around the globe, covering its entire surface in 17 days from 909km up in space.

With three sensors aboard, the new remote sensing satellite beams back an enormous volume of data on diverse aspects of the sea, land and atmosphere. One of the sensors,

MESSR (Multispectral Electronic Self-Scanning Radiometer) senses colors of the sea and land, and recognizes surface features 50m by 50m, utilizing CCD (Charge-Coupled Device) image sensing devices. The MOS-1 is expected to contribute greatly to fishery, agriculture, forestry, resources finding and environment preservation worldwide.

As the prime contractor to the National Space Development Agency of Japan (NASDA), NEC was engaged in system design, system integration and manufacture of key subsystems including major bus subsystems, the MESSR sensor, the DCS (Data Collection System) repeater, ground receiving system and image data processing system.

With more than 30 years of experience in space development, NEC has been involved, as a prime contractor or system integrator, in 23 of the 37 satellites placed in space by Japan.



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NUMBER 138

DIGITALIZATION EXPANDS IN LATIN AMERICA.

In keeping with the ultimate goal of a global ISDN, telecom authorities in Latin America are stepping up their digital network programs.

Telecomunicações Brasileiras S.A. recently awarded NEC do Brasil S.A. a giant order for state-of-the-art digital equipment. It includes NEAX61 digital switching systems (360,000 lines), 5GHz 40M-bit digital microwave communication equipment (1,800 sets), fiber optic communication equipment (200 sets) and PCM transmission equipment (1,300 sets). Most of the systems are to be produced locally with delivery starting this year.

Meanwhile, Empresa Nacional de Telecomunicaciones, Argentina has awarded PECOM-NEC S.A. a contract for NEAX61 digital switches (300,000 lines) and PCM transmission equipment to be installed in the metropolitan and northern areas of Argentina. Local production is scheduled to begin soon. In 1982 NEC constructed a 320-km fiber optic digital telephone system, interconnecting 6 tandem exchanges and 60 telephone offices in the metropolitan area.

NEC is also contributing to the 5-year telecom digitalization project by Compañía Anónima Nacional Teléfonos de Venezuela by supplying NEAX61 digital switches to 97 exchanges in Maracaibo, Puerto La Cruz, and other important areas. For interconnection of these exchanges NEC will supply a 200-km fiber optic communication system.

As one of the world's leading suppliers of digital exchanges, microwave and fiber optic systems, NEC is helping to further the digital revolution throughout the world.

NEW CCD CAMERA STOPS ACTION ELECTRONICALLY.

The trend in color cameras for broadcast use is irrevocably "solid-state". CCD cameras are more compact, dependable and durable than tube types and have no comet tails and burn-in when shooting extremely bright objects.

On top of these inherent benefits, NEC's new SP-3A CCD Color Camera has an exclusive feature—the electronic shutter for fast action. As conventional cameras capture images at a shutter speed equivalent to 1/60th of a second, fast-moving objects are blurred in slow or



still playback on VTR. To remedy this problem, our SP-3A stops the action electronically at 1/60th to 1/2000th of a second, offering precise, clear-cut images.

The SP-3A uses 3 new CCD chips that are anti-smear and -blooming—two for the green channel and one for the combined red/blue channel. This dual green system provides much higher resolution and sensitivity than the conventionally-structured RGB system.

The new CCD camera displays widespread versatility. Besides standalone use it forms an efficient shoot/record system with integral Betacam, MII or 8mm-format VTRs. Options are available

for multi-core or triax remote control.

Users' acceptance of this versatile new camera has been remarkable. NBC, a major U.S. TV network, recently sealed a five-year contract to purchase the SP-3A for electronic news gathering.

A PAL version of NEC's CCD color camera offering broadcast quality will also be released.

WORLD'S FASTEST ECL GATE ARRAYS.

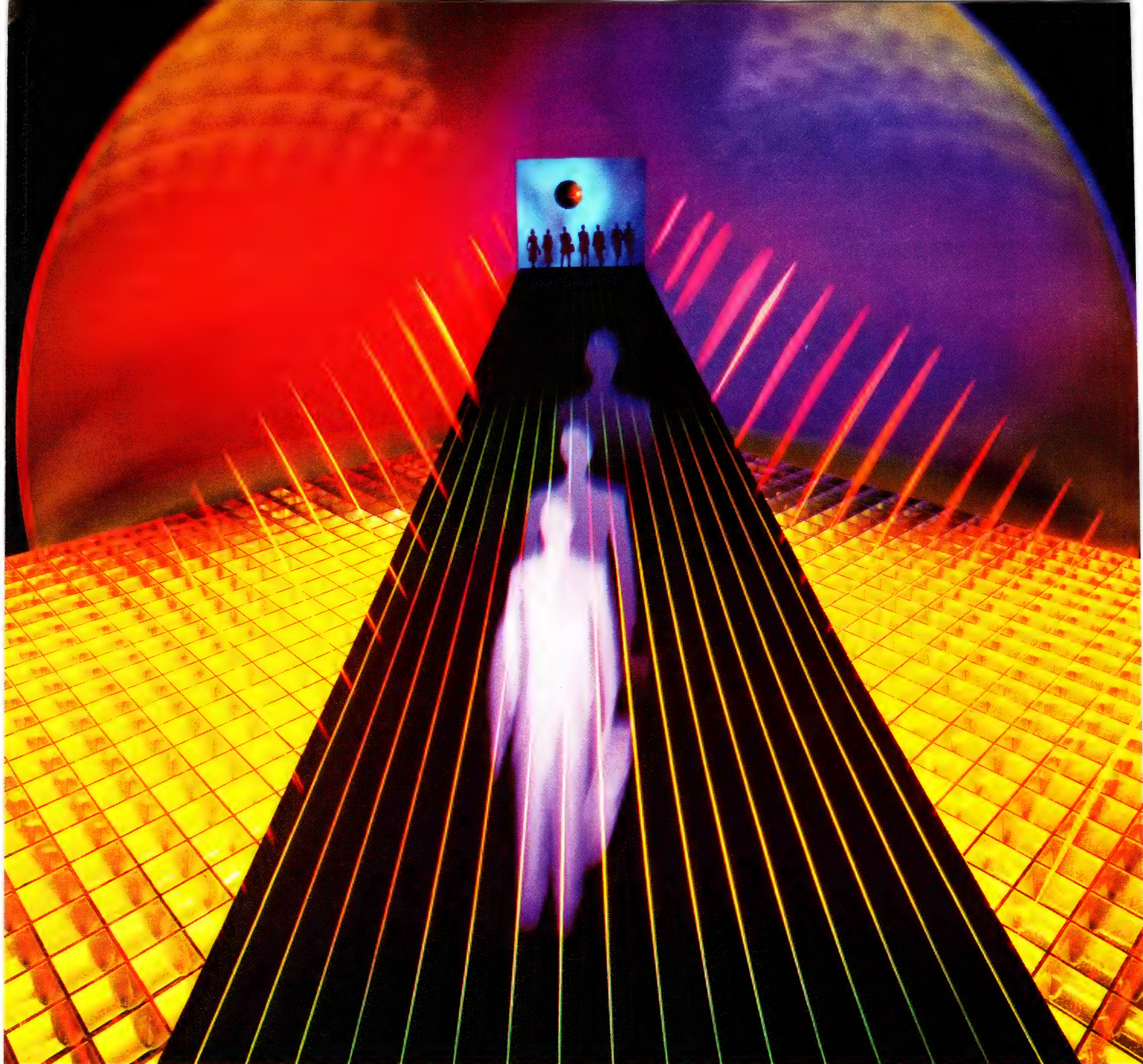
The performance of high-speed silicon logic LSIs is rapidly accelerating. NEC's new ECL-4 gate arrays are the swiftest in the world with a 100ps basic gate delay or 220ps fully loaded.

Combining unprecedented speed and flexibility, the ECL-4 family includes the μ PB6312 with 1,200 gates (400 Full-adders) and the μ PB6303 with 600 gates (200 Full-adders). Both offer 100K or 10KH interface options and ample I/O up to 108 pins.

NEC's ECL-4 gate arrays are available in a choice of 72- or 132-pin PGA packages, and operate in ordinary forced-air-cooling environments since sophisticated heat sinks are standard.

NEC offers 61 internal macros and 33 I/O blocks plus complete CAD tools. The ECL-4 family should hasten the development of speed-oriented computers, graphic terminals, LSI testers and telecom equipment.

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TELECOMMUNICATIONS

SATISFYING THE NEED FOR MORE BANDWIDTH

The telecommunications industry is working toward the advent of the integrated services digital network, the plan to replace the world's analog telephone network with an all-digital net. But until that day arrives—in five years or so—the task is to meet consumer demands for ever more bandwidth. In the coming year, phone companies in the U.S. will be largely relying on the fast-growing T1 and T3 services to meet that goal.

The 1.536-Mbits/s T1 communications link is increasingly popular, especially now that its cost is competitive with the 64-Kbit/s T0 link. Next year industry analysts expect a run on T3, which operates at 44.746 Mbits/s and can therefore provide more voice- and data-communications links. Telephone companies are expected to spend \$600 million on T1 and T3 installation by 1990, up from \$150 million this year, according to Probe Research Inc. in Morristown, N.J.

"Phone companies sweeten the deal [for T3] by charging these large corporate customers a rate on the order of five times the normal T1 rate, but the customer is getting over 30 times the communications

Coming Soon

- Broadband ISDN that will provide business and home users a host of new services
- Bandwidth requirements that will force vast amounts of re-wiring with fiber-optic cable

capability," says Philip Arst, president of Communications Strategies Inc. in Cupertino, Calif. There is also a market for the 6.144-Mbit/s T2 service, which "is four times faster than the T1 link and better suited for the high volume of data being transferred," says Richard LeCour of NTX Communications Corp. in Sunnyvale, Calif.

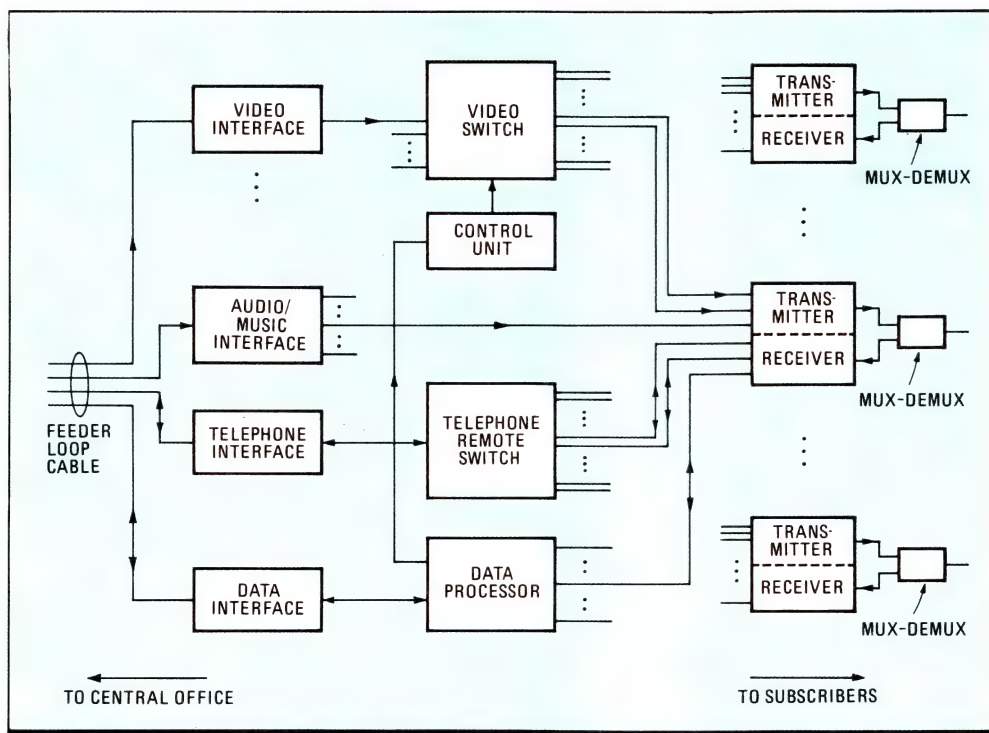
These markets are being stimulated by a welter of new products, notably multiplexing gear, such as the Integrated Network Digital Ex-

change from Network Equipment Technologies Inc. of Redwood City, Calif. "The user with the right multiplexing equipment can get 24 voice-grade lines from one T1 circuit," says analyst Michael De Santis of the brokerage house Alex. Brown & Sons in Baltimore. Another gambit is voice-compression techniques, whereby a single T1 line "can carry up to 90 voice channels," he says.

All of this bandwidth consumption is a foretaste of the day when every business and household will have broadband ISDN, which will run at least 150 Mbits/s, compared with the 64-Kbit/s of narrowband ISDN. B-

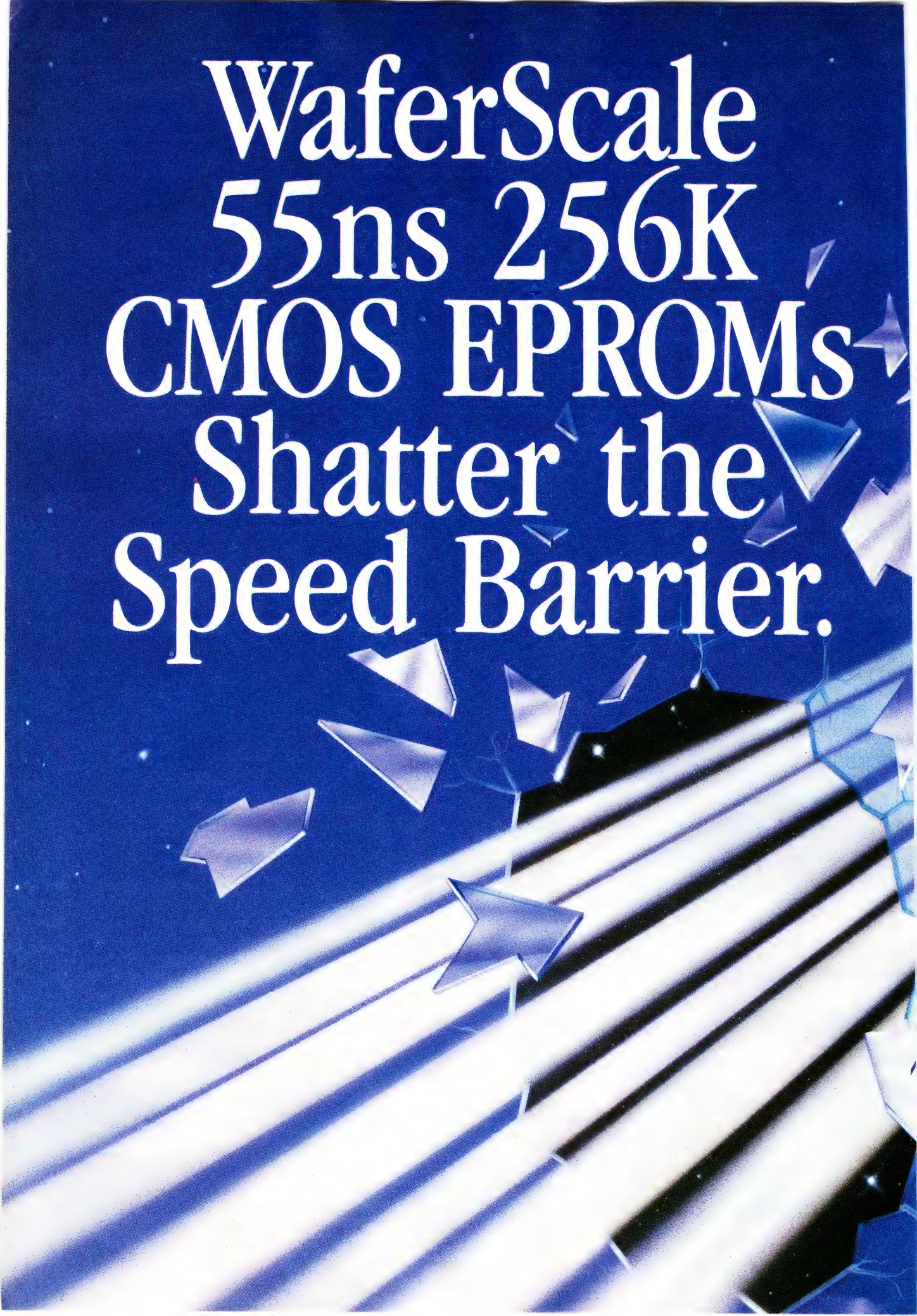
ISDN will give business users access to teleconferencing, large data bases, computer-aided-design and other computer files on demand, and so on. The lure for home users will be video on demand—the ability to request a video product from a library of materials—and other home services, such as interactive videotex and home-security systems.

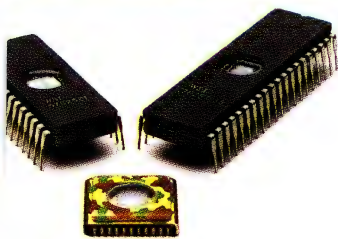
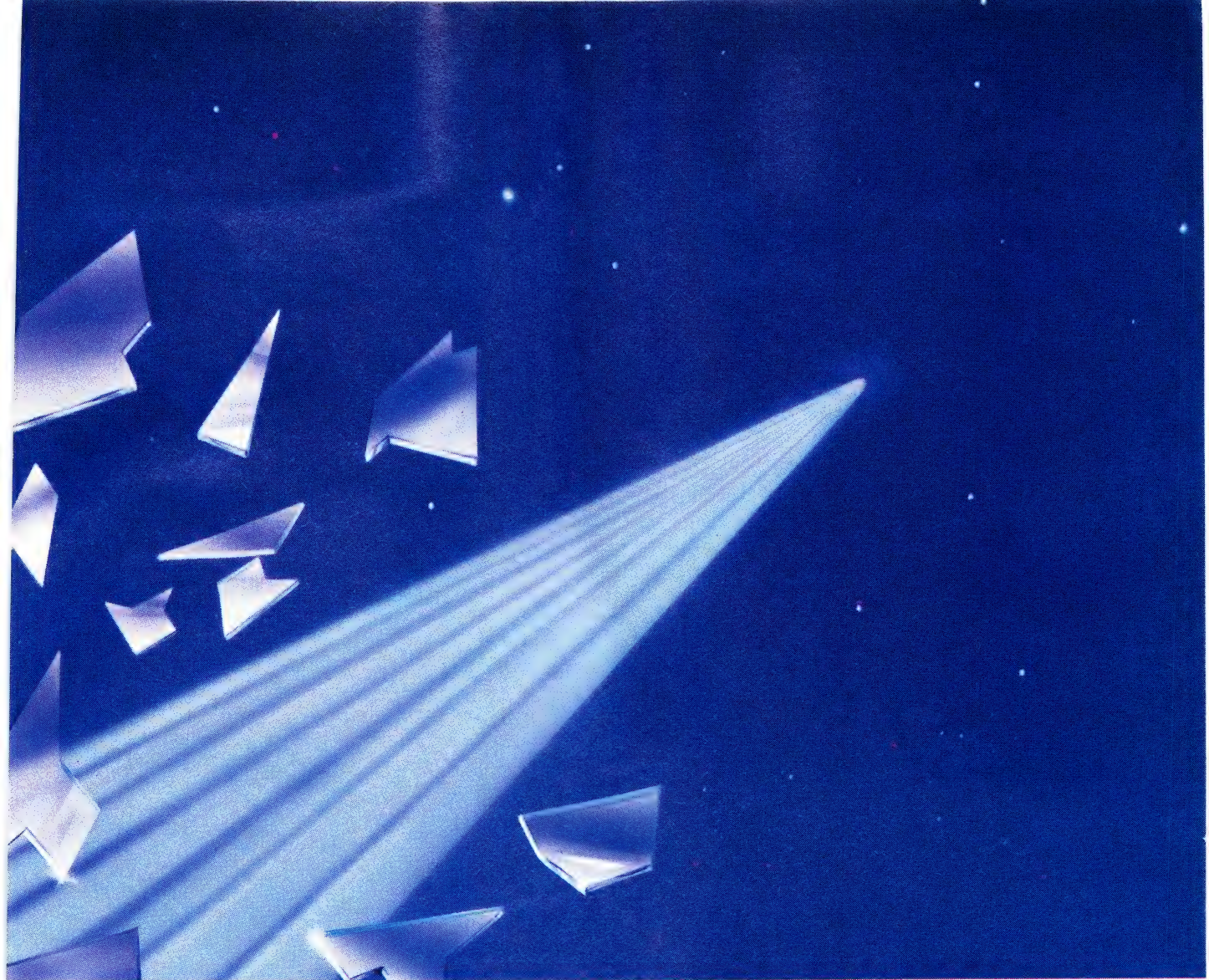
A major stumbling block is the expense of re-wiring subscribers with fiber-optic cable. John Holt, engineering manager for fiber-optics systems at Pacific Bell in San Francisco, reckons that the cost must be cut to no more than \$3,000 to \$4,000 per customer, compared with an estimated \$16,000 today. —Jonah McLeod



BIG BAND. Video-on-demand equipment will need a lot of bandwidth, requiring extensive fiber-optic cabling.

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The background is a deep blue with a diagonal streak of bright, glowing light running from the bottom left towards the top right. Scattered across the scene are numerous sharp, translucent fragments that look like shattered glass or ice, some of which are catching the light and appearing to float or fly through the air. The overall effect is one of high speed and technological breakthrough.



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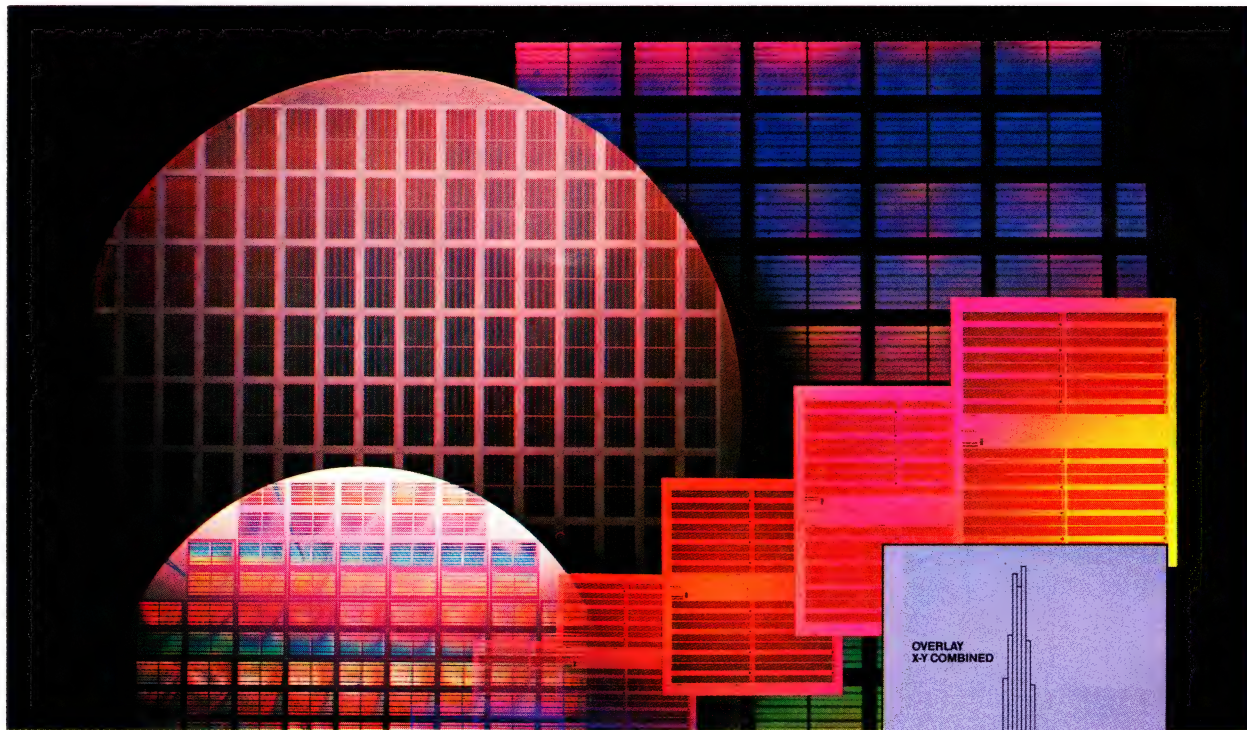
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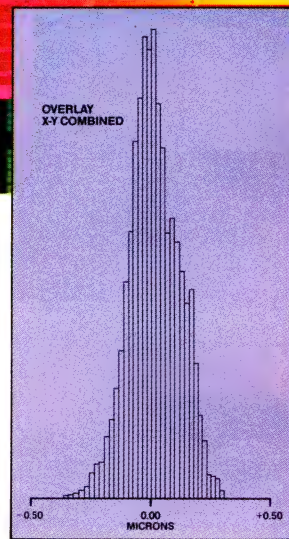


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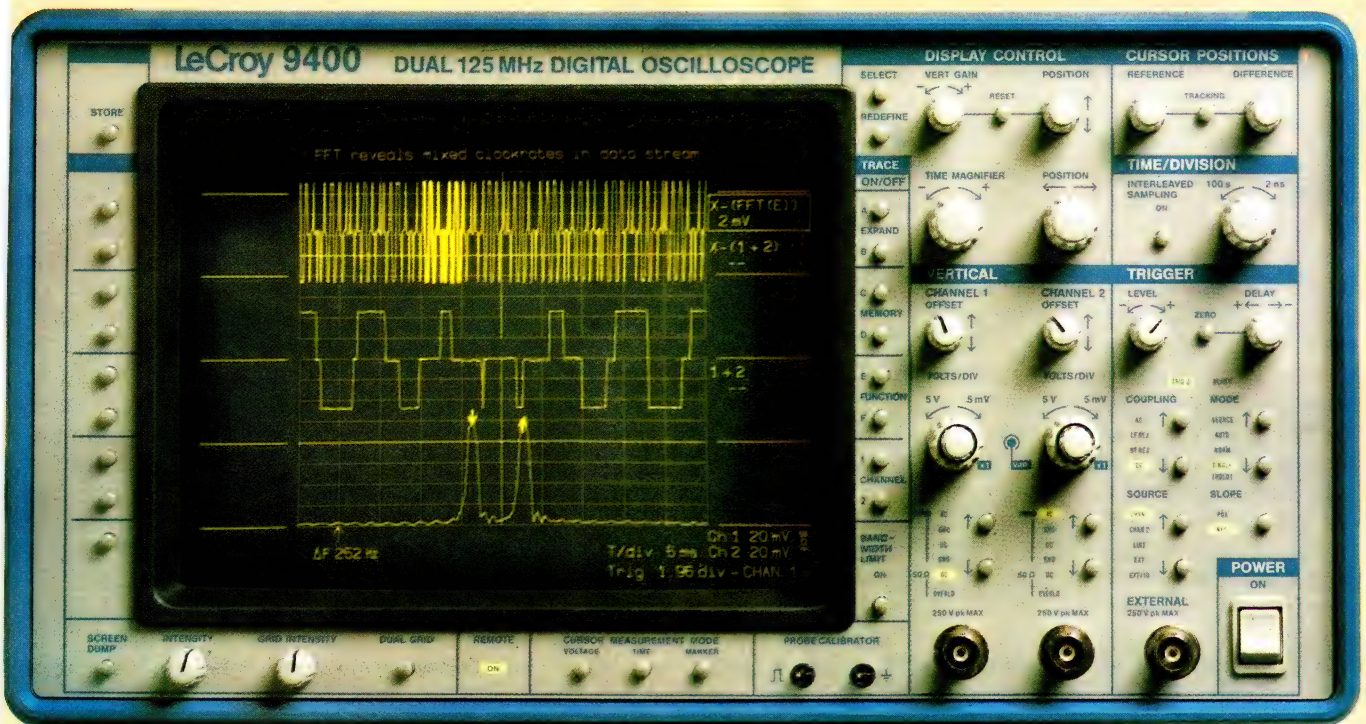


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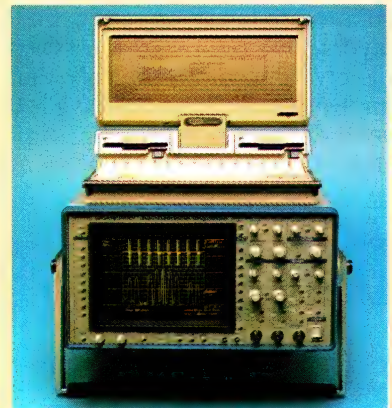
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DATA COMMUNICATIONS

THE DRIVE TO LINK DIVERSE SYSTEMS

Local-area networks have grown so fast and spread so far that the demand among users these days is for help in making sense of it all. "Customers want to be able to run different vendors' communications equipment and software on the same system," says Philip Arst, president of Communications Strategies Inc., Cupertino, Calif. And so the name of the game in 1988 will be multivendor interoperability.

To meet this need, equipment vendors are pledging their support to the International Organization for Standardization's seven-layer Open Systems Interconnection reference model, whenever it finally comes. "Like it or not," says Arst, "any communications-equipment vendor, including IBM Corp., that wants to sell equipment in Europe will have to support the OSI standard when it becomes available, because it will be a legal requirement."

The only problem is that the OSI is only partially implemented, even in Europe. The European standards-setting body for communications, the CCITT, has so far produced protocols for each of the seven OSI layers, but not all of the protocols modules are completely defined. So the collection of protocols thus far implemented does not provide the complete end-to-end solution offered by a proprietary network such as the IBM's SNA (Systems Network Architecture).

Coming Soon

- Products that meet the Open Systems Interconnection model, even if it is incomplete
- Network file systems for personal computers in local-area networks

In the U.S., most network vendors say they intend to adopt the OSI model, once the CCITT modules become complete enough to build a full network. In the meantime, though, vendors are building their own solutions to the problem of linking diverse equipment. One solution that will see much activity in 1988 is the network file system. Long a part of work-station linkups, the systems are just starting to appear in personal-computer LANs.

The application layer of the OSI standard isn't fully defined yet, but it does provide for the network-file-system function. "The trend beginning to appear next year is for various network file systems to be placed on top of TCP/IP [transmission control protocol/internet protocol]," says Subash Bal, vice president of marketing for LAN maker Excelan Inc., San Jose, Calif.

A network file system allows any work station on a network to open and use a file from any other machine in the net. Without such a system, the user would have to copy the file he wanted to access from a distant work station to his own, an approach that propagates multiple copies of files each with its own level of revision. In the work-station arena, the Network File System (NFS) from Sun Microsystems Inc., Mountain View, Calif., has enough popular support that it is now considered a de facto standard.

Until recently, personal-computer nets had no such file-sharing technique. But with more and more personal computers tying into work-station networks, the ability for a PC to support a network file system has become essential.

There are several contenders hoping to cash in on the need for such a standard for PCs. Microsoft Corp. of Bellevue, Wash., is promoting its SMB, or server message-block, network file system; Novell Inc. of Orem, Utah is offering extensions to its Netware product called UNA, for universal network architecture; and Tops (previously Centram Systems West), a Berkeley, Calif., subsidiary of Sun, is promoting its TOPS system. Meanwhile, IBM is promising to roll out its own systems-applications architecture soon. —Jonah McLeod

FROM SNA TO THE OSI STANDARD

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DATA-LINK CONTROL	LAYER 2 DATA LINK	IEEE 802.2	HDLC/LAPB	
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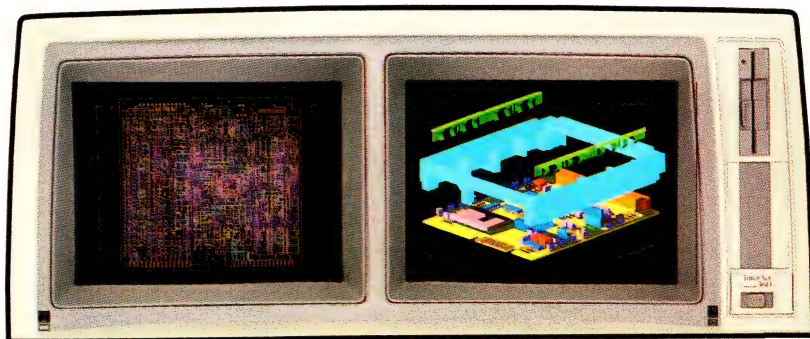
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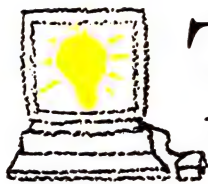
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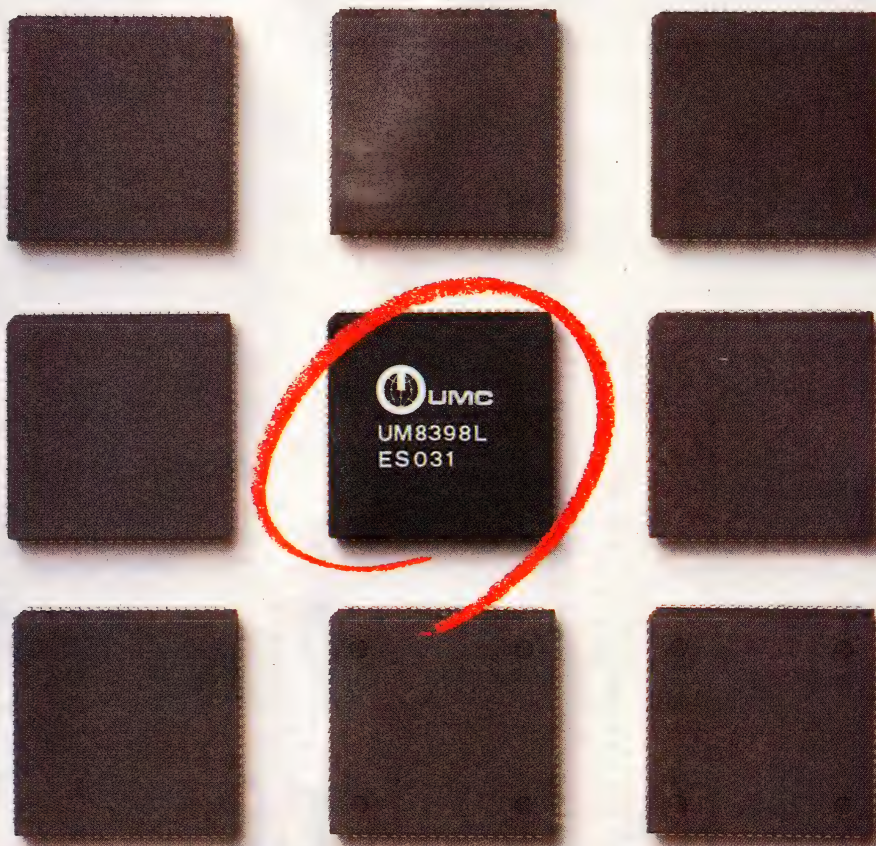
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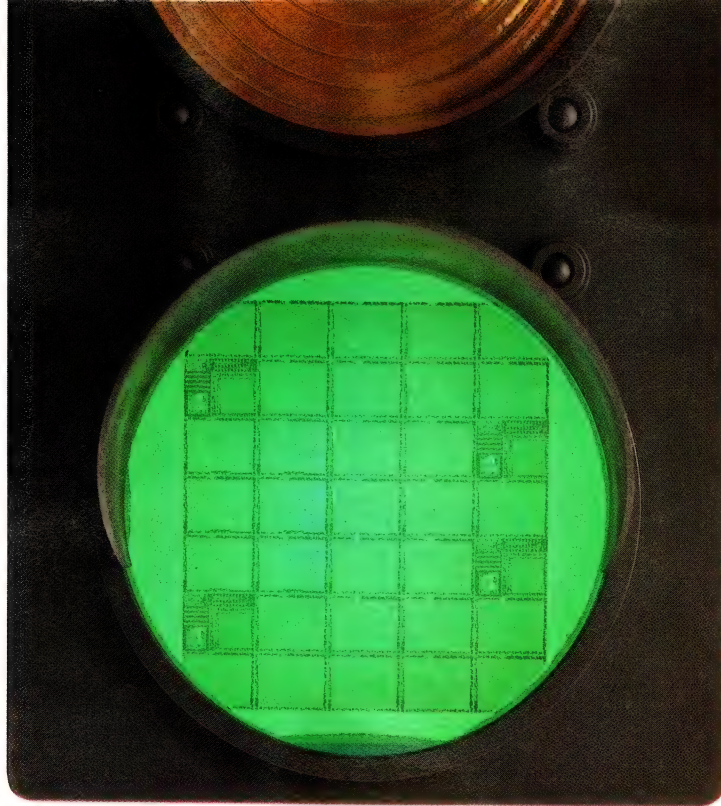
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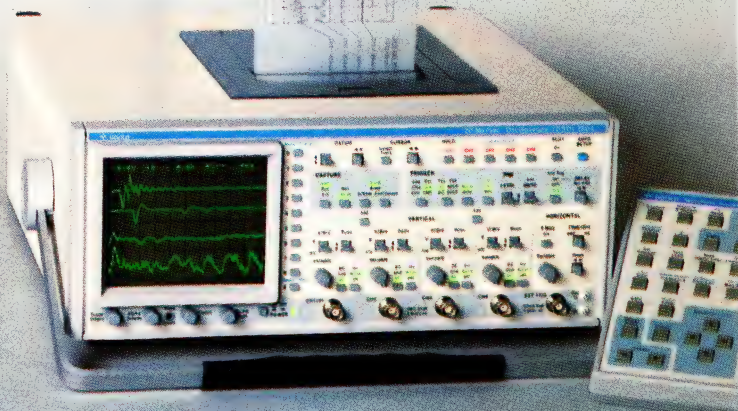
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Electronics

PACKAGING

TRYING TO KEEP UP WITH FAST-MOVING CHIPS

The chip makers' race toward million-gate densities, 500 input/output pins, and 100-MHz performance is driving the packaging industry to new performance heights. The drive to pack more parts and greater performance onto a chip makes it harder than ever for packagers to solve the interrelated problems of size, reliability, and cost. These problems are being addressed with three major packaging thrusts.

Multichip packages are easing the board-space quandary that sometimes results in packaging taking up to 10 times the space of the die itself. At the same time, such packages boost performance and simplify board design. Meanwhile, new printed-circuit-board materials are solving the cross-talk and noise problems that are poised to overwhelm conventional materials. Finally, the emergence of molded-plastic pin-grid arrays is cutting cost-per-pin in half compared with the price of their ceramic counterparts.

At least six major projects are under way using multichip packages that bond several dice to a silicon substrate, connect them with lithographic techniques, and enclose everything in a single package that might be as small as 3 in. square. Multichip packages squeeze dazzling functionality into a smaller space by eliminating the packaging walls between chips. Package-size reductions will approach 5:1 and weight reductions 4:1, industry watchers say. The technology holds significant promise in other areas as well. Since lithographic techniques mean that five 1-mil-wide interconnects can be squeezed into a space now allotted to the narrowest pc-board trace, the number of board layers can be reduced. That, in turn, will cut design time in half. And because fewer solder joints will be subject to thermal stress, reliability will jump by a factor of five.

But not before some problems are overcome. While failures related to thermal stress will be greatly reduced, multichip packages have a built-in reliability problem of their own. Statistically, packaging 50 devices with 99% reliability each can result in package reliability as low as 50%. The solution is using tape-

Coming Soon

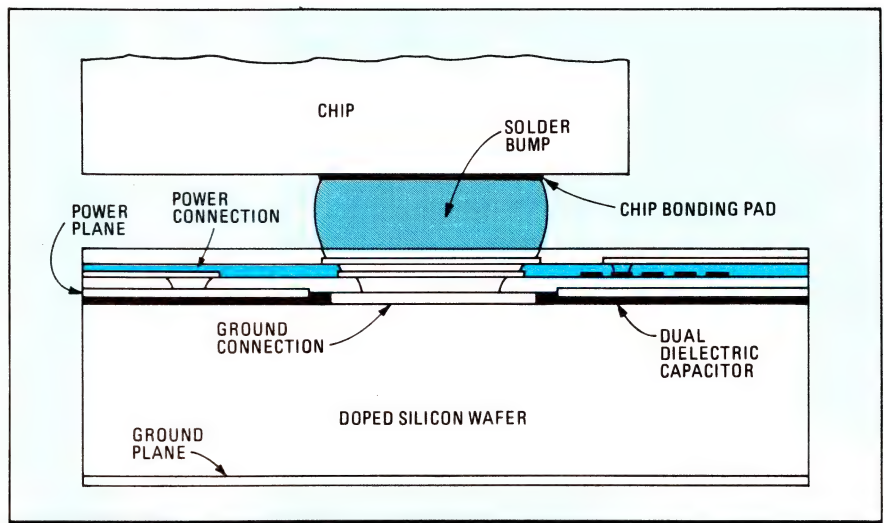
- Multichip packages promise 5-to-1 space savings while delivering higher performance
- Teflon-based boards, immune to noise and cross talk, will handle superchip speeds

automated bonding to test the dice before inclusion in the package, says Robert Wright, manager of Interconnection Technology for Rockwell International Corp. at Cedar Rapids, Iowa. In TAB, bare dice are bonded on tape with leads for testing. Once they pass, all but a nub of the lead is sheared off—just enough is left to bond the die to the silicon substrate.

A prototype being developed at Rensselaer Polytechnic Institute in Troy, N.Y., is squeezing 11 LSI

chips into a shirt-pocket-size package to make a minisupercomputer capable of running at 125 million instructions/s, says John McDonald, a professor in the Electrical, Computer, and Systems Department. The 3.4-by-3.4-cm package is populated with dice fabricated by Tektronix Inc., Beaverton, Ore., in its advanced 1- μ m polysilicon-emitter process. The prototypes are expected to be ready in mid-1988, but commercialization is "not a technology question," says McDonald, "but a matter of dollars and clean rooms—making the technology economical."

Already beyond the prototype stage is AT&T Bell Laboratories' three-chip package implementing Western Electric's WE32100 32-bit microprocessor and its companion memory-management unit and math accelerator [*Electronics*, May 28, 1987, p. 47]. The 1.3-by-3-in. package will enter the market in early 1988. By shortening interconnections, the package eliminates



3 IN 1. Bell Labs integrates three chips—a microprocessor, math accelerator, and memory management unit—into a single package by bonding each circuit directly to a silicon substrate.

propagation delays and lets the module run at higher frequencies—a factor-of-three improvement over surface-mounted packaging of three separate chips for each function, says Charles Bartlett, director of AT&T's Advanced Packaging Design Division in Murray Hill, N. J. Chips are solder-bumped onto substrate and wired into the package, a technology that allows assembling devices with 200 I/O pins operating up to 100 MHz and boasting under-2-ns rise times. Other multichip-package players include Mosaic Systems, Troy, Mich.; the Semiconductor Research Corp. at Auburn University, Auburn, Ala.; and Hitachi in Japan.

While silicon-on-silicon irons out the technology wrinkles, the 4:1 price advantage of molded-plastic over ceramic pin-grid arrays should gobble up the high-lead count market, particularly for application-specific ICs. Typically, ceramic arrays cost 6¢ to 8¢ per pin, but chip makers have been willing to pay the price in return for power dissipations up to 10 W. Interconnection Solutions Inc. has changed all that with a new molded—not laminated—package. Because pins are molded into the body of the package, it's equally possible to inexpensively mold in details such as heat sinks [*Electronics*, February 19, 1987, p. 39].

The method, based on polyimide plastic, "is a unique combination of existing technologies," says Bill Werther, vice president of engineering. "We treat the materials to get them to stick to each other and

cure the package to reduce heat stress." The packages, ranging up to 400 pins in size, will be in production by the end of the year, says Werther.

Of course, packaging extends beyond chips. In printed-circuit boards, materials interacting with high-performance components create spurious signals in the present generation of G10 epoxy glass material. New materials, with superior electrical properties and mechanical properties equal to G10, are needed, says Robert Wachob, director of marketing for Rogers Corp.

The Rogers, Conn., company's solution is a new material, R02800, based on Teflon to which proprietary fillers have been added. It can handle chips with rise times as steep as 30 ps without generating significant noise or cross talk—a twentyfold improvement over standard epoxy-glass boards. Teflon's electrical properties are well known and it has been used in microwave applications for a decade. But its 224 coefficient of thermal expansion—which made for high stress among components as the board warmed or cooled—has kept it from use in pc boards. But R02800's coefficient of 24 creates little stress on solder joints, which is important in multilayer boards, says Wachob.

The material is 10 times more expensive than conventional epoxy glass, but since material accounts for a relatively small part of the finished board, the cost disadvantage diminishes when processing, shaping, and other aspects are included. —Jack Shandle

CHIP PROCESSING

'FINE TUNING' OPTICAL STEPPERS

Conventional photolithography is periodically dismissed as a chip-making technology nearing obsolescence. But it still ranks as the solid first choice of volume device makers around the world, and continuous improvements in optically based machines have kept up with the push for density and speed, and the consequent move to ever-smaller feature sizes.

As a result, photolithography has attained a longevity few would have predicted three years ago. At that time, it seemed that more exotic techniques such as electron-beam and X-ray lithography would have to be perfected to break the 1- μ m barrier and beyond. But in fact, optically based machines will be the workhorses in manufacturing the first submicron generation of integrated circuits that is just starting to appear.

"We believe that in processing down from 1 to 0.5 μ m, optolithography now has the ability to take us through the [technology] generations," says Pallab K.

Coming Soon

- Better light sources and trilevel resists for submicron optical lithography
- Masked ion-beam tools, promising high throughput and resolution within 0.25 μ m

Chatterjee, director of Texas Instruments Inc.'s Semiconductor Process and Design Center in Dallas and Semiconductor Group vice president. A series of improvements now in sight for optical step-and-repeat units supports this posture. Most of them involve fine tuning for commercial production many of the advances demonstrated in the lab, consultants say.

Adding more intense mercury light sources, for example, can push resolution ever smaller, and I-

line steppers—whose mercury lamps have a 354-nm wavelength—are among the newest ways of accomplishing this. Another advance is phasing in trilevel resists as a replacement for single-level resists, for use in the highest-density areas of circuits.

But the next step in chip processing is far from clear. Over the next few years, manufacturers will have to settle on a proven production technology that will handle devices fabricated with 0.5- μ m design rules and smaller. Major IC producers are still study-

ing the alternatives, and they are far from unanimous in making a final choice, industry analysts say. A favorite candidate of many observers is direct-write electron-beam lithography, which entered the limelight via the Department of Defense's Very High Speed Integrated Circuit program.

But early performance troubles with Perkin-Elmer Corp.'s Aeble 150, built for VHSIC Phase 2 production, has contributed to doubts about e-beam's commercial potential. So far, direct-write e-beam has been used mostly for small-run gallium arsenide designs, where the precision advantage of the technology suits it for gates with dimensions down to 0.25 μm . E-beam's main debit is low throughput, with resulting yield and cost problems. Despite the claims that Aeble 150-type e-beams can produce up to 30 four-in. wafers an hour—a figure competitive with optical steppers—in practice the rates have been less than 10 wafers, most sources agree.

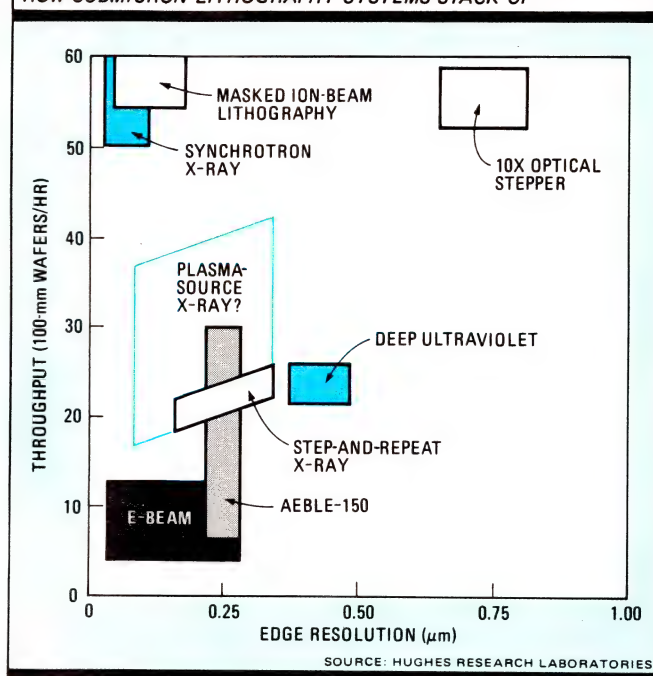
This is not a handicap with application-specific ICs, however, which generally are produced in low volumes and with fast turnaround times. Proponents are trumpeting e-beams as the next equipment of choice for ASICs, which could be the majority semiconductor type by the 1990s. But skepticism still abounds. Richard C. Henderson, manager of the Silicon IC Dept. at GMHE/Hughes Aircraft Co.'s Research Laboratories, is doubtful about upping yields and lowering costs. The problem could be solved by teaming an e-beam equipment supplier with a heavyweight device manufacturer, "but no U.S. company is making the effort," he says. His Malibu, Calif., lab, a major center of research into semiconductor processing, developed the e-beam design that became the Aeble 150.

E-BEAMS FOR ASICs?

Surprisingly, this downbeat assessment is echoed by a major e-beam supplier, Japan's JEOL, whose \$3.5 million model 683 is a principal competitor of the similarly priced Aeble 150. "We see no e-beam sales to ASIC production," says Michael Hassel Shearer, product manager for e-beam and ion-beam lithography at JEOL's U.S. operation in Peabody, Mass. He predicts that the technology will stay largely confined to specialty production, primarily GaAs, unless a clear economic advantage emerges. This has not occurred even in Japan, where JEOL alone has installed some 25 e-beam units. Industry consultant Jerry D. Hutcheson concurs, and can spot "no dramatic new push occurring in e-beam." President of VLSI Research Inc. in San Jose, Calif., he downplays throughput as the main barrier. "The real killer is price," he says. "Only the military or the largest ASIC manufacturer can afford e-beam."

Market consultant Dataquest Inc., also in San Jose, takes a similarly restrained view, but analyst Joseph Grenier thinks the throughput issue "might be a crossable barrier if a very high-throughput machine is developed." Beyond that is another hurdle, he says, "which is psychological—the reluctance to change." Grenier and others believe that IBM Corp.—which has been operating some 40 e-beam machines for years, primarily for fast-turnaround prototyping—could pro-

HOW SUBMICRON LITHOGRAPHY SYSTEMS STACK UP



vide impetus to the technology. "They have vast direct-write experience and incredible capacity in the area, but have not chosen to share it," says Grenier.

The only e-beam/ASIC program of consequence has surfaced at European Silicon Structures, which is using an Aeble 150, but few details have been revealed. Perkin-Elmer's Charles Biechler, vice president and general manager of the Electron Beam Technical Division in Hayward, Calif., says the European concern finds an economic advantage in manufacturing 10-level CMOS devices. "We believe strongly that when this success becomes more visible to competitors, they are going to have no choice but to emulate it," he says.

If not e-beam, then what other semiconductor line-making technologies have solid possibilities to take over at 0.5 μm ? X-ray lithography's chances, strong a few years ago, have declined sharply, particularly at leading U.S. research-and-design organizations, although strong efforts continue in Europe and Japan. TI's Chatterjee believes that at 0.5- μm and maybe down to 0.4- μm , "the use of excimer-laser lithography is going to be adequate." At Hughes Research Laboratories, John L. Bartelt says masked ion-beam lithography, invented at Hughes in 1974, offers better submicron resolution and higher throughput capability. He cites recent innovations in mask technology, ion optics, mask/wafer alignment, and step-and-repeat stages, which have resulted in a prototype system that demonstrates throughput of up to 60 four-in. wafers per hour with 0.1- μm alignment and 0.1- μm resolution. "Masked ion-beam lithography is suitable for any of the process technologies, from 0.5 μm down to 0.25 μm ," says Bartelt, manager of the Ion Physics Department. Hughes does not build semiconductor equipment for the commercial marketplace, but is considering a licensing agreement. —Larry Waller

Which core materials keep their cool in



Copper-Clad Invar

High density surface mounting of leadless ceramic chip carriers has created new thermal and mechanical problems for those working on high reliability electronic projects.

More and more companies are addressing these problems by incorporating metal cores as thermal mounting platforms in their printed circuit board assemblies. The choice of metal laminate comes down to two: Copper-Clad Molybdenum or Copper-Clad Invar. Both do an equally good job of solving the problem of the coefficient of thermal expansion

(CTE) mismatch between chip carrier and substrate. But, that's where the similarity ends.

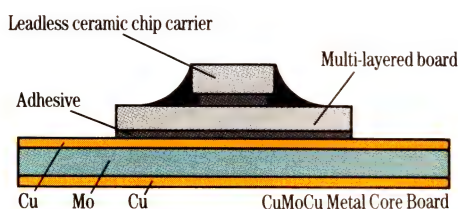
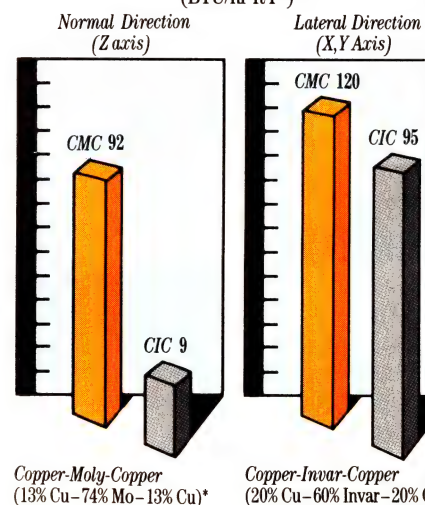
Dissipating the heat.

Higher packaging densities create higher watt densities. Dissipating this heat can be as critical as matching the CTE of an assembly. The thermal conductivity of Copper-Clad Molybdenum is comparable to aluminum and much

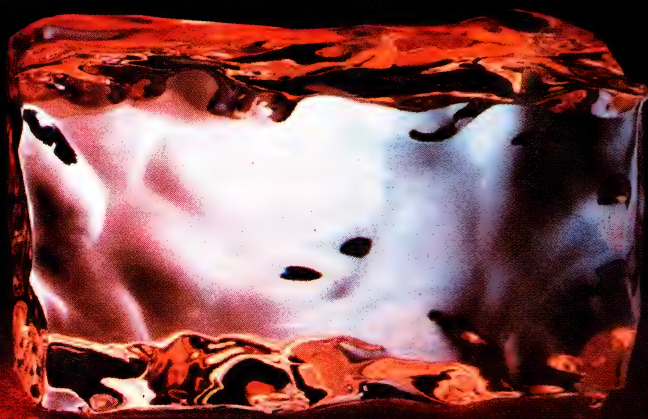
higher than Copper-Clad Invar, making it a superior heat sink. Compared to Copper-Clad Invar, Copper-Clad Molybdenum is

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Comparison of Thermal Conductivity (BTU/hr-ft F°)



Material helps LCCC's in heated situations?

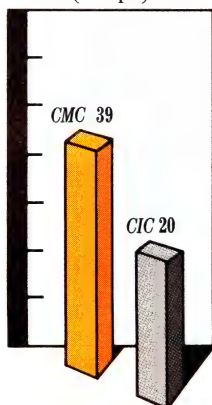


Copper-Clad Molybdenum

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Solder joint failures also can be caused by vibration, shock, and flexure. Copper-Clad Molybdenum has a much higher modulus of elasticity than Copper-Clad Invar. A core of Copper-Clad Molybdenum provides maximum rigidity to the chip carrier assembly.

Comparison of Modulus of Elasticity ($\times 10^6$ psi)



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For some applications, magnetic susceptibility is a design consideration. Molybdenum is only slightly paramagnetic (4×10^{-6} emu/g), whereas, Invar is a ferromagnetic material (100+ emu/g).

*The necessity for equivalent CTE's is the criterion for comparison.

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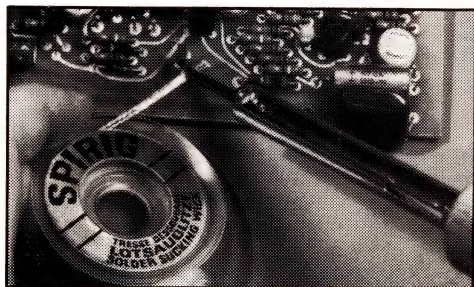
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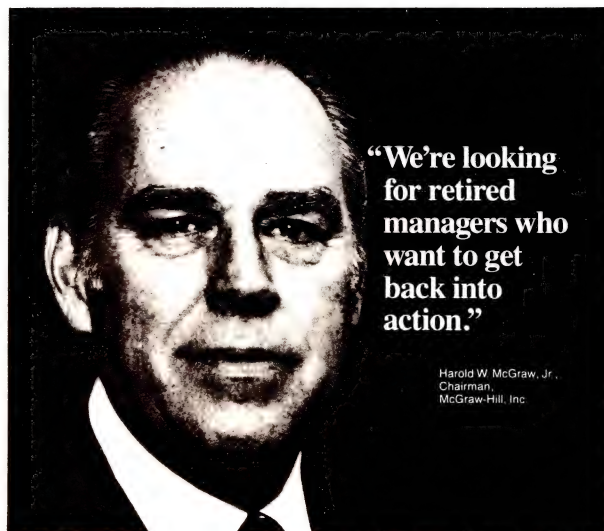
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FACTORY AUTOMATION

IS 1988 FINALLY THE YEAR FOR MAP?

A major swing to the Manufacturing Automation Protocol has been forecast for years, but it could finally happen in 1988 when version 3.0 of the factory-automation protocol is set to make its long-awaited appearance.

Next year will also see a continuing march of microprocessors and personal computers into the factory, as well as software that provides for better parts and process tracking. Expert systems will also be on the rise, as will more vision-guided robots, industry watchers predict.

"The biggest trend in factory automation is more of the same," sums up Laura Conigliaro, an analyst at Prudential-Bache Capital Funding in New York. "Computers are getting smaller and more powerful and are finding their way into everything. And as distributed processing comes more and more into its own, that means everything has to get connected through networks."

Just what kind of networks those will be remains an open question. MAP backers hope that the debut of version 3.0 products late next year will help push the protocol off dead center. As a standard that permits programmable devices from multiple vendors to communicate, eliminating so-called "islands of automation," MAP holds great promise. But despite a worldwide effort by more than 200 companies to push the technology, MAP has been slow to catch on outside of General Motors Corp., which originated the concept.

Coming Soon

- MAP version 3.0 products that may move the protocol into manufacturing's mainstream
- More automated inspection and test systems linked with the manufacturing process

"We've got a lot of clients who are playing around with a pilot MAP network, but none of them are planning for full-scale implementation," says James C. Weinberg, a Chicago partner at Peat Marwick Main & Co., which does factory-automation consulting. The reason, he says, is "cost and the lack of final standards."

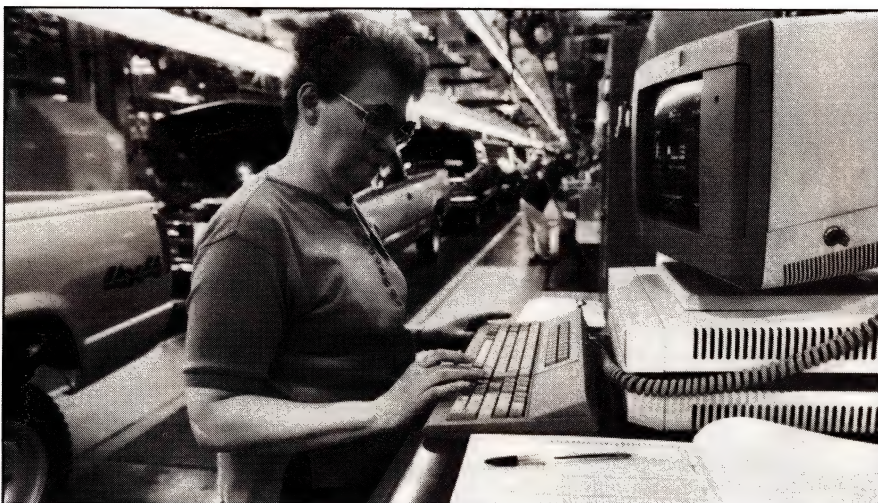
Indeed, a full-blown MAP broadband network implementing all seven layers of the Open Systems Interconnect architecture can cost

anywhere from \$3,000 to \$15,000 per node, says Robert S. Crowder, president of Ship Star Associates, a Newark, Del., network consulting firm. By contrast, a typical factory Ethernet installation goes for \$700 to \$800 per node, Crowder says. What's more, MAP implementations must be done in the current 2.1 version. And while several vendors offer products aimed at easing the transition from 2.1 to version 3.0, many users are wary of installing a MAP net that would be obsolete by 1989, industry watchers say.

The final MAP 3.0 specification is due by June, and backers are hoping for a quick product blitz to get volume moving and push prices downward. The most optimistic hope to see manufacturers installing MAP 3.0 networks before 1988 is over. "I think there's a good chance that by the fourth quarter of next year we'll have a respectable number of vendors with products that can interoperate," says Charles J. Gardner, an Eastman Kodak Co. executive who chairs the MAP/TOP Users Group Steering Committee. Others aren't so sure. "The real impact will be in 1989," says J. Tracy O'Rourke, president and chief executive officer at Allen-Bradley Co., Milwaukee.

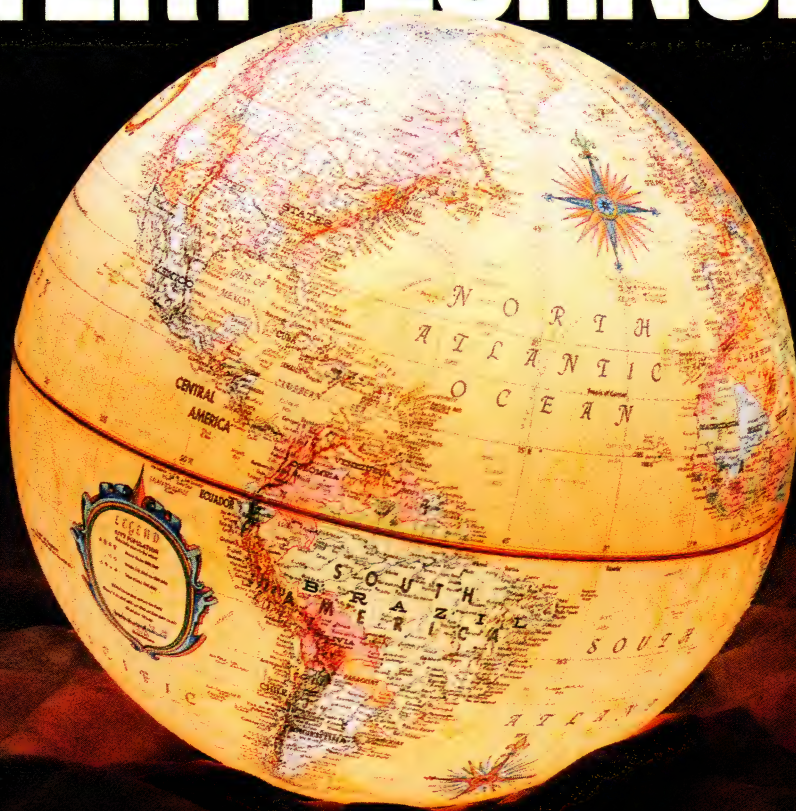
Most experts expect good news on other fronts. Peat Marwick's Weinberg, for example, anticipates the increased use of automated inspection and test systems that are linked with the manufacturing process to achieve adaptive process control. He also foresees "a big explosion in use of expert systems in some areas." Likewise, noncontact sensing in applications such as automatic bar-code parts-tracking systems is expected to get bigger play.

—Wesley R. Iversen



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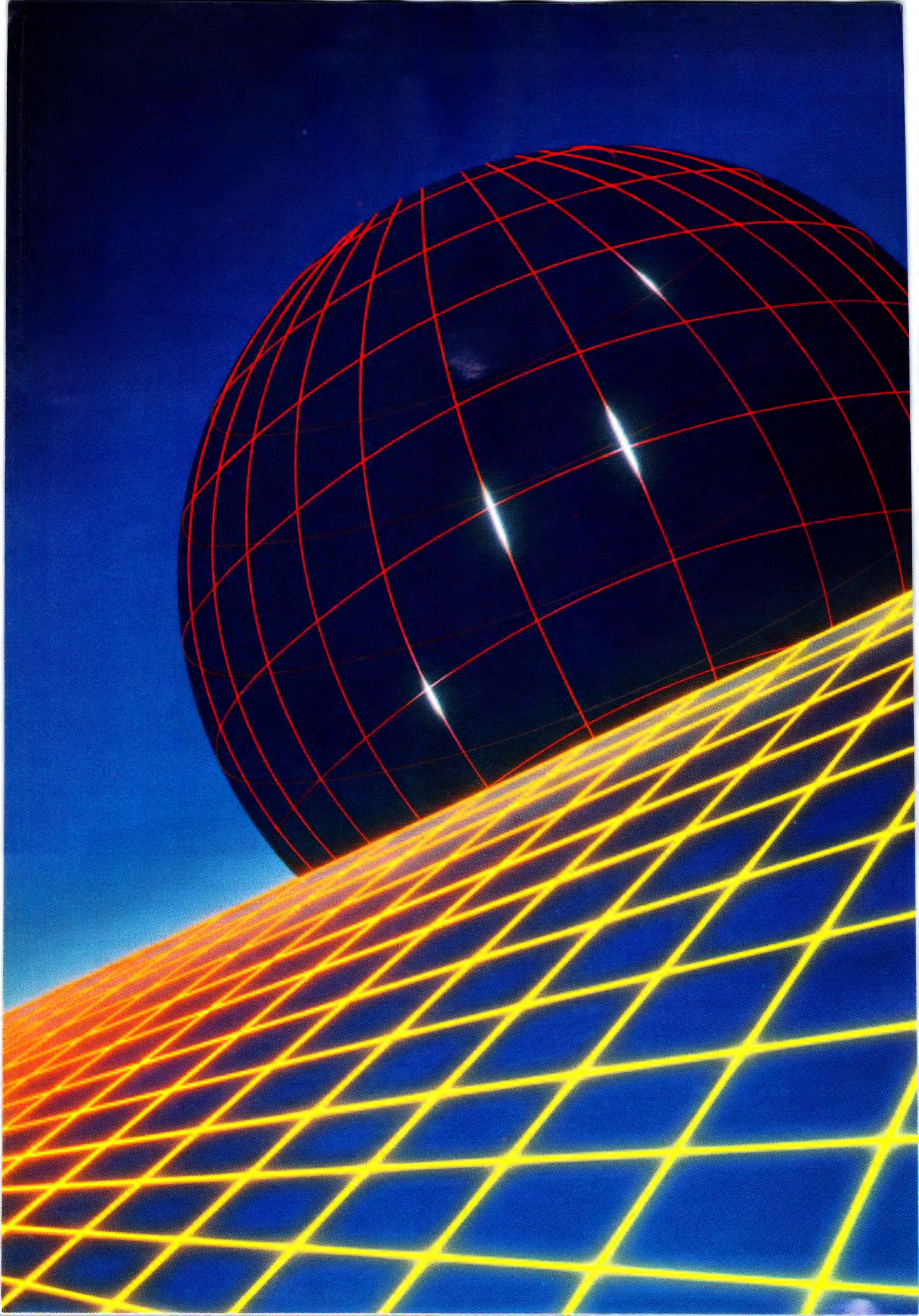
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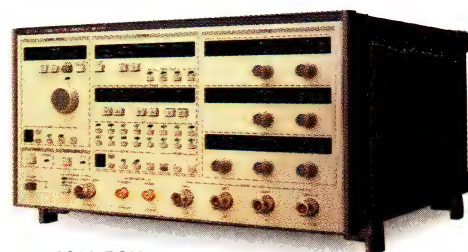
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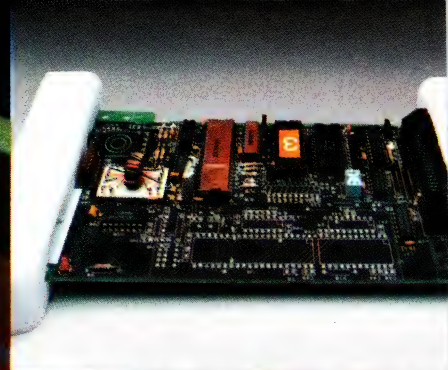
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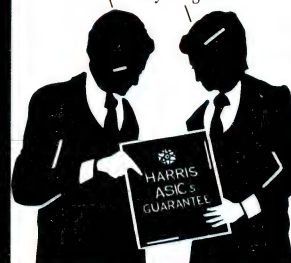
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MILITARY/AEROSPACE NEWSLETTER

AIR FORCE TO TRY AMORPHOUS-SILICON, ACTIVE-MATRIX LCD

The Air Force wants to see if liquid-crystal displays with an active matrix of amorphous silicon can outperform electroluminescent displays in the rugged, portable flight-line computers that will be part of its Integrated Maintenance Information System program. The search has led to Ovonic Imaging Systems Inc., which will develop two 6-by-8-in. flat-panel displays for the Air Force Human Resources Laboratory at Wright-Patterson Air Force Base in Ohio. If the Troy, Mich., company meets its goals, the 640-by-480-pixel active-matrix displays will draw only 1 W to 1.5 W of power—roughly 3% of what a comparable EL display requires—while maintaining about the same resolution, 80 pixels/in. Further, the Ovonic Imaging displays will feature a 90° viewing angle—compared to about 60° degrees for EL—with a 20-to-1 contrast ratio that is comparable to EL. IMIS is being considered for use on the next-generation Advanced Tactical Fighter. □

EIA: GROWTH IN DEFENSE-ELECTRONICS SPENDING IS LEVELING OFF

The electronic content of U. S. defense work, including procurement and research and development, is beginning to level off after six years of fast and steady growth, according to the Electronics Industries Association. The Defense Department now spends some \$53 billion, or about 40% of its annual budget, in these categories. In its annual 10-year forecast for the defense-electronics market, the EIA predicts that this proportion will hold steady at or near the 40% level through 1997. Overall, EIA forecasters look for defense spending to decline slightly until it bottoms out in 1992. They expect, however, that spending will then begin to rise at about 1% a year. R&D funding, they say, will remain at its present peak through 1988. As for the Strategic Defense Initiative, the EIA says spending will stay in the \$3.5 billion to \$4 billion per year range through 1997. □

CUSTOMS ADDS MORE RADAR BALLOONS TO SPOT DRUG SMUGGLERS

The U. S. Customs Service will add half a dozen tethered radar balloons to the one it is now operating to spot low-flying planes and surface vessels smuggling drugs into the U. S. One of the new balloons will flesh out the coverage in the Caribbean, where a single aerostat is now stationed over Grand Bahama Island, while the others will be deployed over the next two years along the southern border of the U. S. The first will go up in early November from Fort Huachuca, Ariz. The new balloons, supplied by Westinghouse Electric Corp. Defense and Electronics Systems Co. of Baltimore, cost \$15 million each and carry a modified Westinghouse AN/TPS-63 radar at altitudes to 15,000 ft. Data from the radar is transmitted to Customs Service ground stations. □

FROM THOMSON, A DIGITAL DISPLAY MAP FOR FRENCH TACTICAL AIRCRAFT

Thomson-CSF is developing a high-speed digital map system for the Tactical Combat Aircraft, the French equivalent to the U. S. Advanced Tactical Fighter. The system will store 150,000 square miles of mapped terrain on 5¼-in. optical disks, offers 512-by-512-pixel full-color resolution, is powered by a custom microprocessor, and has a 60-Hz noninterlaced refresh rate, says Patrick Berniolles, an engineering manager with Thomson's Aerospace Group in Issy-Les-Moulineaux, France. Called Dracar, the system is optimized for ground-collision avoidance, and key to that will be the next step in Thomson's development work: completion of a display mode that, by providing a digitized perspective view of the terrain, will help pilots keep their craft low to the ground and below enemy radar, Berniolles says. □

MILITARY/AEROSPACE NEWSLETTER

VTI AND VITESSE TO MELD SILICON AND GALLIUM-ARSENIDE DESIGN

Military-chip designers are starting to press for gallium-arsenide design tools, says Douglas G. Fairbairn, vice president and general manager of the ASIC Division of VLSI Technology Inc. So the San Jose, Calif., company has joined with Vitesse Electronics Corp. to create a design environment enabling semicustom-chip users to complete early phases of designs before selecting either technology. Depending upon speed and power-dissipation requirements, designs could then be implemented in either GaAs or silicon CMOS. GaAs-chip maker Vitesse of Camarillo, Calif., will develop the new library with interfaces to existing CMOS-design software from VLSI Technology. This fall, Vitesse will deploy a GaAs library of small- and medium-scale integration functions. By next summer, the library will work with VLSI Technology's compilers, allowing for either silicon CMOS or GaAs chips, says Patrick L. Hoffpauir, executive vice president at Vitesse. □

BIPOLAR-DEVICE ARRAY COMES TO THE AID OF AGING SYSTEMS...

Aging military systems that rely on obsolete components will now be easier to maintain, thanks to a generic bipolar device array developed by Honeywell Inc.'s Solid State Electronics Division, Colorado Springs, Colo. The chip can be customized to emulate devices that are now out of date, such as diode transistor logic. It measures 70 mils on a side, integrates 200 transistors, 14 capacitors, and 8 resistor arrays, and is built in a 5- μ m bipolar process. Honeywell is currently working on eight application-specific designs for the Sacramento Air Logistics Command at McClellan Air Force Base in California, which sponsored the chip's development. Honeywell and Air Force officials will discuss the device at the Government Microcircuit Applications Conference in Orlando, Fla., late this month. □

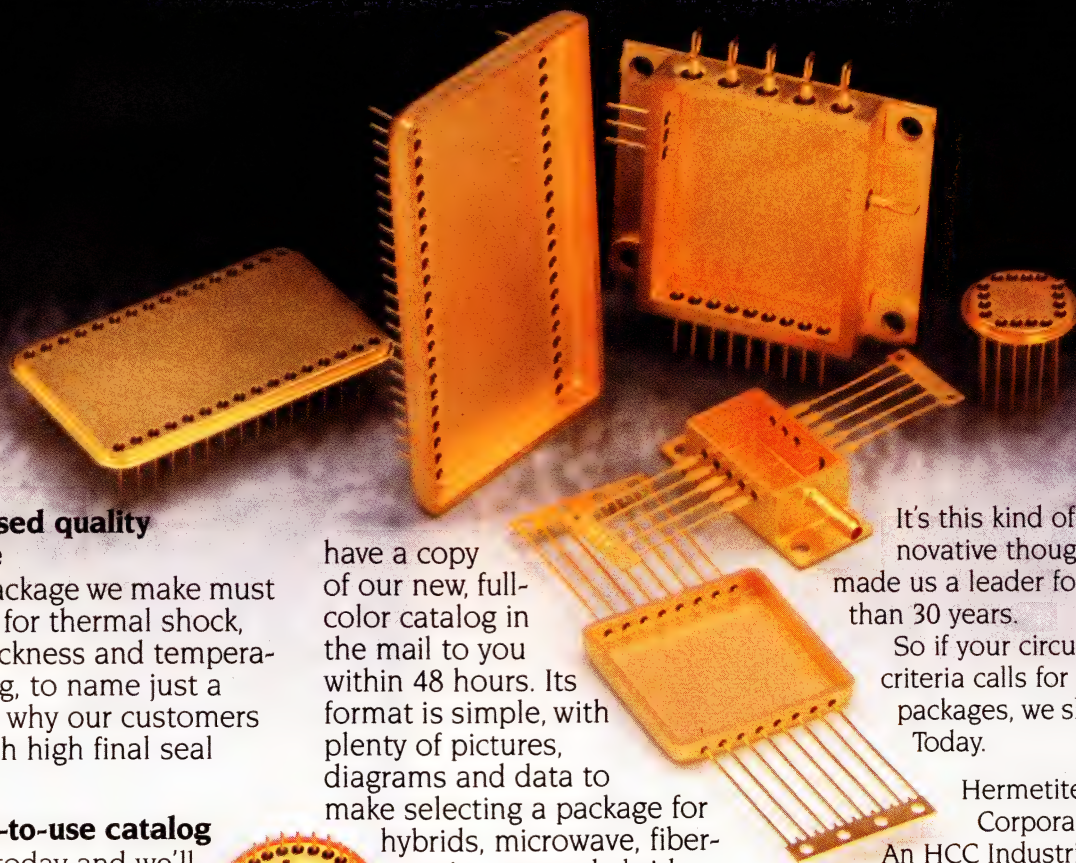
...AND EMULATORS FILL IN FOR EARLY '60s IBM COMPUTERS

The Air Force has decided not to buy new hardware—which would engender the huge cost of rewriting software—to replace the IBM Corp. 1800 computer systems installed in the early 1960s for maintenance of the Minuteman missile-guidance unit. Instead, the service has ordered 32 emulators worth \$5 million from Cable & Computer Technology Inc., an Anaheim, Calif., firm specializing in computer emulators. The systems, to be delivered over the next year, will be designed around Advanced Micro Devices Inc.'s 2910 bit-slice microprocessors and built with commercial parts and peripherals. Interest in emulation systems is high—this is the fifth emulation award CCT has won in the past year from the Air Force and the Navy. □

TRW SATELLITE LASER TRANSCEIVER WILL SPOT TERRESTRIAL SIGNALS

Improved gallium-aluminum-arsenide diodes are the key to a direct-detection laser transceiver for a satellite that will demonstrate new laser-communications technology early in the 1990s under a joint project of the Air Force and the National Aeronautics and Space Administration. Work on the space-borne equipment is under way at TRW Inc.'s Electronics and Defense Sector in Redondo Beach, Calif. The transceiver will detect a laser signal from the ground or from orbiting vehicles and transmit a variety of signals, including high-resolution TV. Its three main elements, all based on the same GaAs diode technology, are a laser transmitter, a receiver, and an experimental electronic package. In addition, the transceiver unit will carry a diffraction-limited optical assembly that TRW says is "essentially a 7.8-in.-diameter laser telescope." Test data will be transmitted at rates ranging from 1.72 to 220 Mbits/s, using an 870-nm laser beam. □

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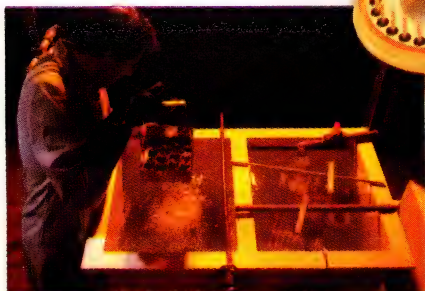
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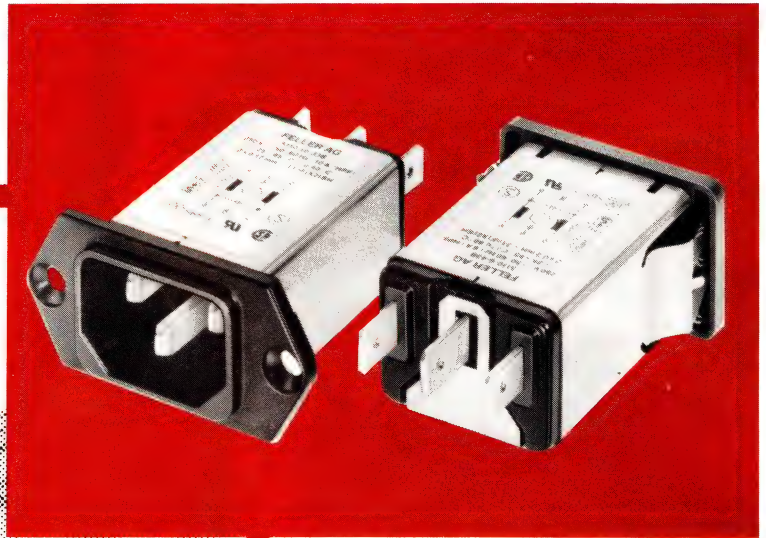
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NEW PRODUCTS

ADAPTER BOARDS LINK IBM'S PS/2 TO 32 DUMB TERMINALS

HOSTESS SERIES ALSO DOES DATA ACQUISITION OVER MICRO CHANNEL

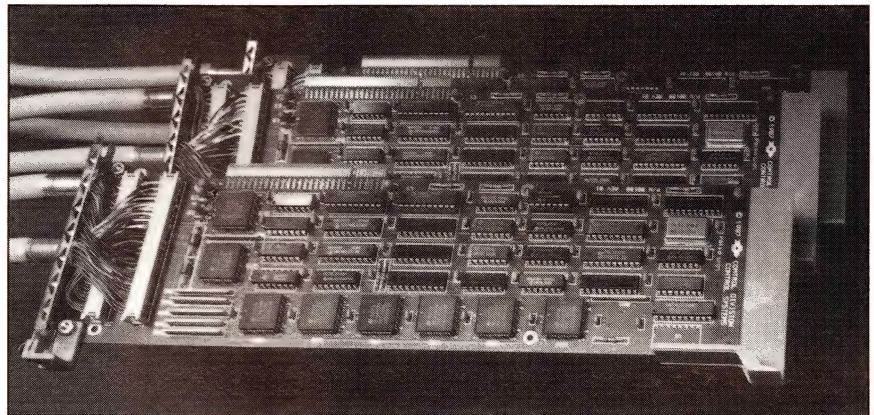
Users of the IBM Corp. Personal System/2 now can leverage the machine's processing power in multiuser, data-acquisition and simple networking applications. They can add four or eight serial ports for each PS/2 expansion slot with Control's series of multiport-adaptor boards designed to work with the PS/2's Micro Channel bus.

The St. Paul, Minn., division of Control Systems Inc. had a head start: its new Hostess/MC, Hostess 550/MC, and the Smart Hostess/MC perform the same functions as its five-year-old Hostess multiport serial adapters for IBM's Personal Computers. The new line targets three primary applications: multiuser systems that link up to 32 terminals to the PS/2; data-acquisition systems that use the PS/2 to take sensor data over serial lines; and simple star networks that link multiple PS/2s for low-speed file or peripheral sharing.

ADDED PORTS. "There's been a need for additional serial ports with the PC-bus products—and with the speed and the power of the PS/2, it simply means that the need for serial ports will be even greater," says Walter J. Stull, Control's general manager. "Our Hostess/MC products will enable users to take advantage of what the PS/2 has to offer." Control's boards offer a range of price and performance, including a data-communications microcontroller on the top-of-the-line unit.

Similar multiport serial adapter boards for the PS/2 are also under development by other companies. Arnet Corp., Nashville, Tenn., for example, plans first shipments in the fourth quarter of an eight-port board known as Multiport, a company executive says. An 80186-based eight-port version known as Smartport is planned for shipment in next year's first quarter.

At the low end of Control's line, the Hostess/MC will provide an economical, nonintelligent multiport capability based on one 8250 universal-asynchronous transmitter/receiver per port. Each Hostess/MC port can be set for baud rates from 50 to 56,000 bits/s. But system constraints dictate that multiuser systems will be limited to three to five si-



TRIPLE THREAT. Hostess boards add four or eight ports to PS/2 computers for multiuser systems with up to 32 terminals, for data-acquisition, or for star networks.

multaneous users with each port running asynchronously at a typical 9,600-baud rate, Stull says. A four-port Hostess/MC is priced at \$595 in single units, while an eight-port version goes for \$895. The board will be available in November.

For users who need better asynchronous performance, the Hostess 550/MC ups the ante by relying on 16550 UARTs. The 16550s provide 16 bytes of first-in-first-out buffering where the 8250 UARTs handle only 1-byte transmissions in each direction between processor interrupts, says Stull. This capability will improve throughput because fewer interrupts are required. The Hostess 550/MC is expected to handle up to eight simultaneous users at 9,600 baud per port, Stull says. It will be available in December. In single units, it is priced at \$695 and \$1,095 for four- and eight-port versions, respectively.

For applications requiring maximum throughput, the Smart Hostess/MC adds an Intel 80186 processor running at 8 MHz to offload data-communications tasks from the PS/2 processor. This board is generally expected to support simultaneous use by 16 or more people with ports set at 9,600 baud, Stull says. But high-end operating systems such as The Santa Cruz Operation Inc.'s SCO Xenix can support up to 32 users. The use of an 8530 USART in each port means the Smart Hostess/MC can han-

dle synchronous communications based on such protocols as SNA, SDLC, or X.25, as well as asynchronous terminals.

The Smart Hostess/MC incorporates as much as 512 Kbytes of random-access memory, half of which can be dual-ported for memory sharing between the PS/2 processor and the on-board 80186. As many as 128 Kbytes of erasable programmable read-only memory can also be included, enabling original-equipment manufacturers and end users to add customized firmware.

FOUR OR EIGHT. The Smart Hostess/MC will be available in production quantities next March. Final pricing has not yet been set, but for single units it will be under \$2,000 for an eight-port board, and under \$1,600 for a four-port.

All three Control boards offer a range of interface choices: RS-232-C, RS-422, RS-485, or current-loop. The serial ports themselves are contained in an exterior housing that can be mounted on the back of the PS/2 or used as a freestanding unit. Optional connector types can be DB25, DB9, or RJ45. The Control boards require no switches or jumpers to be set. A 3½-in. diskette containing software that allows addresses and interrupts to be set using a screen menu is supplied with each board.

— Wesley R. Iversen

Control Division, Control Systems Inc., P. O. Box 64750, St. Paul, Minn. 55164. Phone (800) 826-4281 [Circle 340]

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Storage capacity varies from 55 to 100



to 150 to 200 Mbytes among the eight models. Data-transfer rates range from 5 to 10 Mbyte/s. The SCSI and EDSI interfaces are available only on the 200-Mbyte models.

Evaluation units will be available in the first quarter of 1988 with production quantities coming on the market by mid-year. In volume purchases, the drives will cost from \$5 to \$8 per Mbyte.

Control Data Corp., 8100 34th Ave. South, Minneapolis, MN 55440

Phone (612) 853-3600 [Circle 348]

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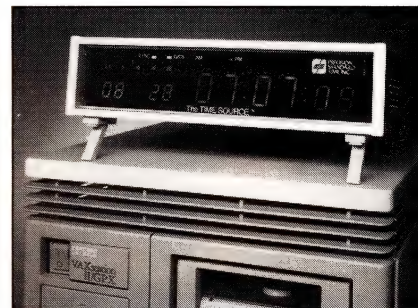
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The Time Source timing device from Precision Standard Time Inc. eliminates inadvertent data loss and event-coordination errors on computer networks by providing a clock-calendar accurate to within 10 ms.

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Kbit/s RS-232-C interface. Since Time Source is not a clock, it cannot drift or become less accurate, and since it reads time from a broadcast, two units will always agree.

Available now with a 72-hour backup battery and VMS-compatible software, the Time Source costs \$1,495.

Precision Standard Time Inc., 105 Fourier Ave., Fremont, Calif. 94539.

Phone (415) 656-4447 [Circle 345]

MULTIBUS II BOARD RUNS AT 32 MBYTES/S

Concurrent Technologies Inc.'s M-CP 386/016 single-board computer uses an Intel Corp. 80386 processor running at 16 MHz to attain 32 Mbytes/s data rates.

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Expansion space is provided on the board for Intel's 80387 floating-point coprocessor and up to 1 Mbyte of erasable programmable read-only memory with an additional eight slots supporting up to 1 Mbyte of zero-wait-state RAM.

Memory capacity can be further extended by adding one or two memory-expansion modules of either 4 or 8 Mbytes. Available in November, the M-CP 386/016 costs \$4,950.

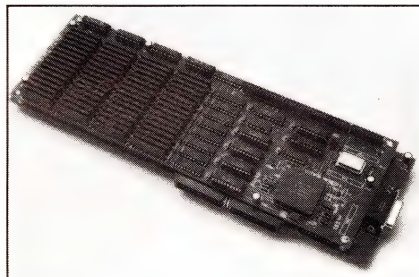
Concurrent Technologies Inc., 25401 Cabot Rd., Laguna Hills, Calif. 92653.

Phone (714) 768-3332 [Circle 346]

COLOR BOARD PUTS CAD/CAM IN MAC II

Manufacturers of high-resolution computer-aided design systems can now deliver 16 million colors and 1,024-by-768-pixel resolution on Apple Computer Inc.'s Macintosh II by integrating RasterOps Corp.'s Colorboard 1/104.

The board offers more than double



the 640-by-480-pixel resolution of the Mac II and many times the Mac II's 256 colors. The Colorboard achieves true color capability by assigning 24 bits per pixel and implements it with 2.5 Mbits of video random-access memory.

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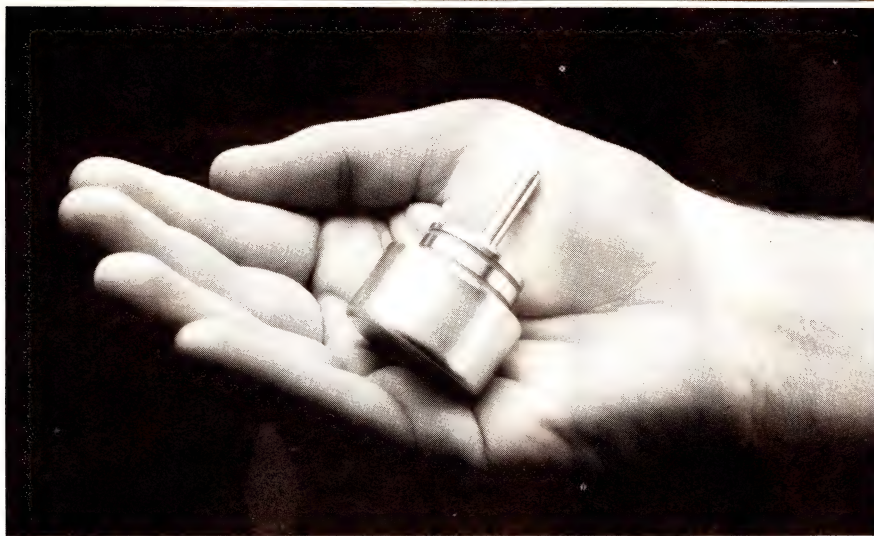
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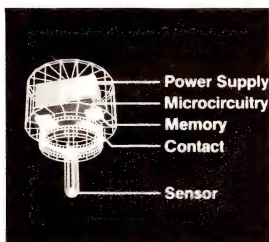
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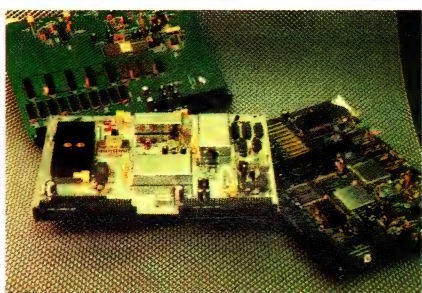
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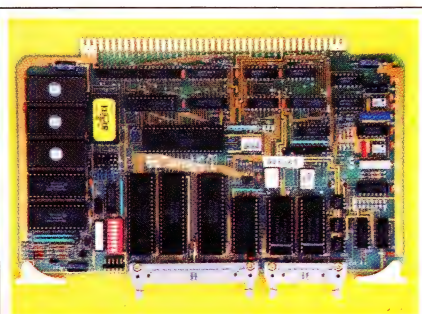
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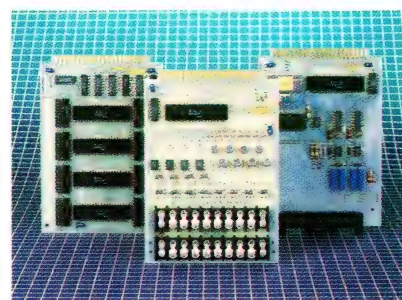
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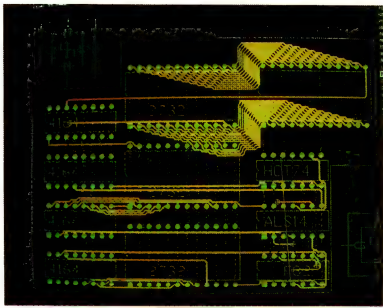
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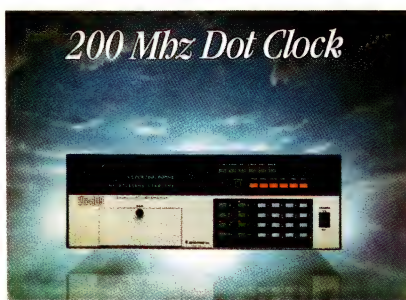


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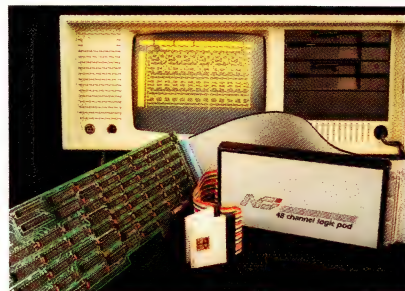
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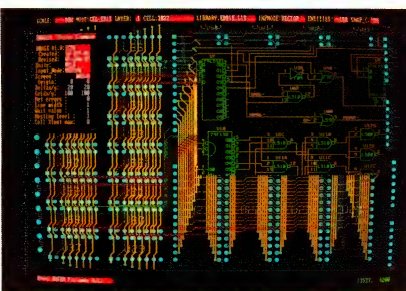
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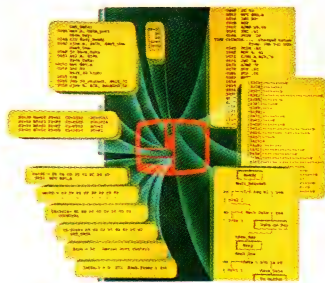


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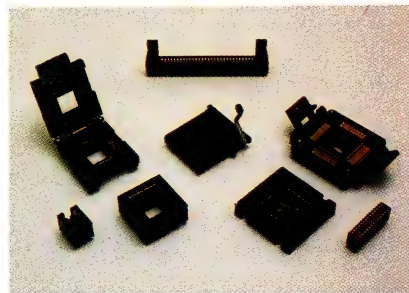
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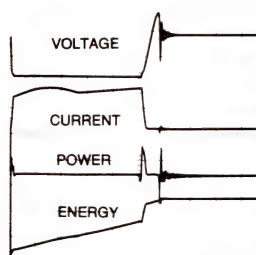


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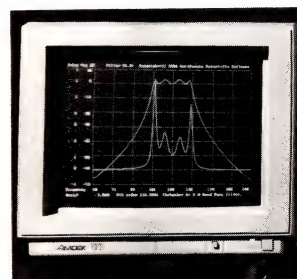
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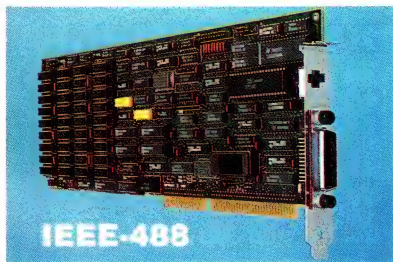
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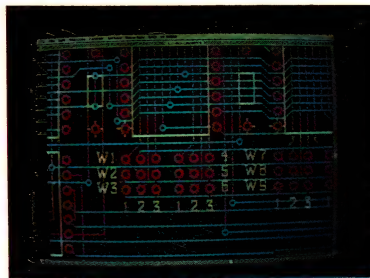
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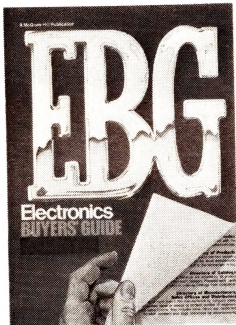
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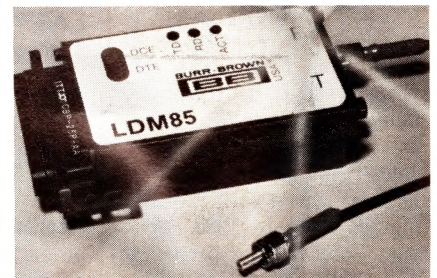
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ELECTRONICS WEEK

CHIP SALES MAY HIT \$45 BILLION IN 1990

Global semiconductor sales will hit \$45 billion in 1990, a jump of \$18.6 billion over 1986, according to the annual forecast of the Semiconductor Industry Association in Cupertino, Calif. The SIA projects that the strongest annual percentage growth will come this year, with chip sales rising 21.8% to \$32.1 billion, compared with \$26.4 billion in 1986. In 1988, world chip sales are expected to rise 17.9% to \$37.8 billion. The SIA predicts slower growth in 1989, with sales rising only 7.5% to \$40.7 billion. After this slight slump will come an 11.2% rise to \$45.2 billion in sales in 1990, the association says.

SILICON COMPILERS AND SUN SIGN PACT

In a multimillion-dollar agreement, Silicon Compiler Systems will offer its Genesil systems design software on technical work stations from Sun Microsystems Inc. of Mountain View, Calif. The San Jose, Calif., company will also buy about \$3 million worth of Sun work stations for software development and support.

BATTELLE DESIGNS LOW-COST COUPLER

Battelle of Columbus, Ohio, has devised a technique that could produce couplers for plastic optical fibers for as little as \$2, compared with the \$100 to \$200 for glass-fiber couplers. Plastic-fiber couplers have been scarce because these fibers, now used mainly in medical sensors, until recently have been a high-loss medium, says a Battelle researcher, Tony Boiarski. He foresees plastic fibers extending into other short-distance uses such as local-area networks and automobiles. The Battelle coupler has a multimode optical waveguide circuit that can be

reproduced by the hundreds on a flat surface by ultraviolet lithography. NTT Corp. in Japan is devising a similar process to make glass-fiber couplers, Boiarski says.

LATTICE EMERGES FROM CHAPTER 11

Lattice Semiconductor Corp. has emerged from Chapter 11 bankruptcy 88 days after filing for it last July. What's more, the Beaverton, Ore., company turned in the best product revenues in its history, totaling nearly \$3 million for the quarter ended Sept. 26. Lattice executives believe the company will reach the break-even point, with sales rising another 25%, before the end of the year. Raymond P. Capece, executive vice president and chief operating officer, attributes the turnaround to lower costs—the work force is now 75 people, down from 175 a year ago—and increased revenues from programmable logic, which now accounts for 75% of Lattice's sales.

CONVEX JOINS APOLLO NETWORK

In its third such deal in the past two months, Apollo Computer Inc. of Chelmsford, Mass., has signed on supercomputer maker Convex Computer Corp. of Richardson, Texas, to its Network Computing System. The two companies will jointly market Convex's C1 supercomputers with Apollo's work stations in a distributed multivendor network. With their combined networking, graphics, and computing clout, the firms are targeting technical applications in areas such as circuit simulation, image processing, and artificial intelligence.

CCITT SPLITS ON ERROR CONTROL

Standards for the error-control protocol for switched-network-protocol modems are

still being worked out by Study Group XVI of the Consultative Committee on International Telephony and Telegraphy. At a late-September meeting in Geneva, the committee split into two factions. On one side were Belgium, France, Germany, Italy, the Netherlands, and Sweden, as well as IBM Europe, all voting for the Microcom Networking Protocol. The United Kingdom and Japan, however, support a modified version of the Link Access Protocol. The CCITT agreed that whatever the outcome, the future standard should include MNP error control, be compatible with MNP protocol modems, and also include a LAP-based protocol.

LOCKHEED TO BUILD BATTLEFIELD SYSTEM

Lockheed Electronics Co. of Plainfield, N.J., is developing an advanced electronic battlefield communications system that will enable the U.S. Army to rapidly exchange tactical information on interactive computer displays, which would link armor units on the battlefield. Under a \$270,000 subcontract from SRI International, of Menlo Park, Calif., Lockheed is developing software on Sun 3/160 work stations, which will be compatible with SRI and other contractors' software.

SEMATECH CHIEF MAY BE INSIDER

The search firm looking for a chief executive officer for the Sematech consortium has a green light to interview top managers at member companies. Sematech booster Irwin Federman, a vice president at Advanced Micro Devices Inc., also says a plan is in the works to require about half of the workers at the chip-manufacturing-technology cooperative—700 running at full strength—to come from member companies, with employees serving two-year stints at the consortium.

FIBERS TRANSMIT SATELLITE SIGNALS

Field tests using optical fibers to transmit satellite signals show that the material is more effective than coaxial cable, says Bell Communications Research, Redbank, N.J. Bellcore researchers linked 115,000 ft of fiber cable to a 21-ft C-band satellite antenna dish and were able to maintain high-quality signals at microwave frequencies over the entire cable length. By contrast, signals traveling through coaxial cable tend to degrade beyond 800 ft., Bellcore says.

IBM'S ROLM TO OFFER ITS LARGEST PBX YET

Rolm, the telecommunications subsidiary of IBM Corp., has gone to market with a new generation of modular business-communications systems, the IBM 9750 and 8750. The hardware is built around a computer-controlled branch exchange that can expand customer systems from 100 to 20,000 voice and data lines. The capacity is 70% larger than previous Rolm CBX systems. Future releases of the IBM systems 9750 and 8750 will support the integrated services digital network.

MICROSOFT, LOTUS IN SOFTWARE WAR

Microsoft Corp., of Redmond, Wash., has launched a major challenge to Lotus Development Corp., of Cambridge, Mass., in the IBM personal-computer spreadsheet market. Microsoft's PC Excel has major advantages over Lotus 1-2-3, the most popular spreadsheet by far. Excel is designed to take better advantage of the power of high-end PCs, and Microsoft's multitasking Windows software links it to other programs running at the same time. Excel also has built-in facilities that make it easy for 1-2-3 users to learn.

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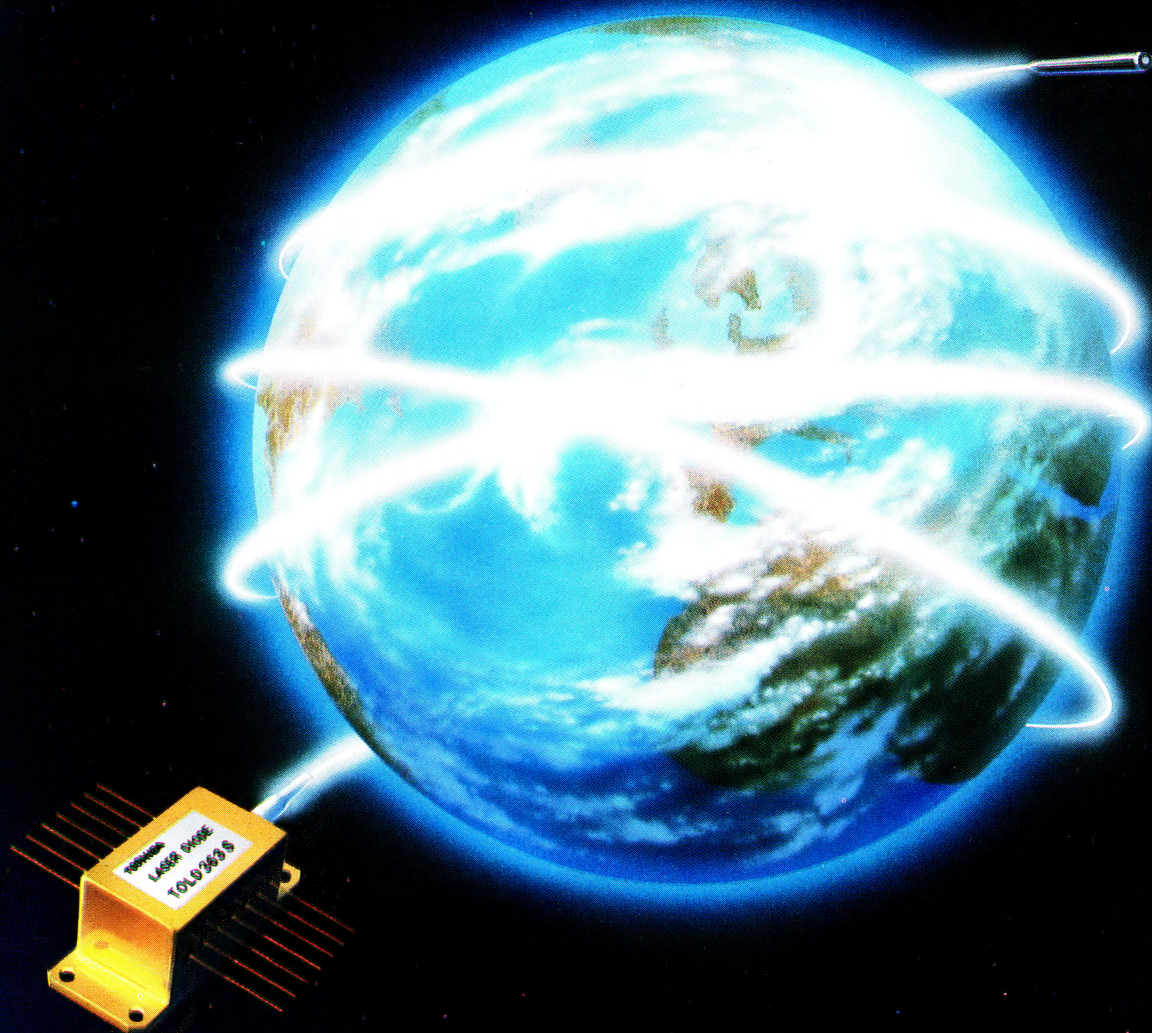
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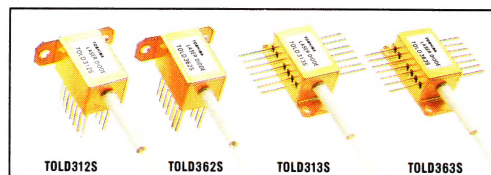


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